SG390 Series
RF Signal Generators

SG392 (DC to 2.025 GHz)
SG394 (DC to 4.050 GHz)
SG396 (DC to 6.075 GHz)

User Manual

Stanford Research Systems

Revision 1.03

Certification

Stanford Research Systems certifies that this product met its published specifications at the time of shipment.

Warranty

This Stanford Research Systems product is warranted against defects in materials and workmanship for a period of one (1) year from the date of shipment.

Service

For warranty service or repair, this product must be returned to a Stanford Research Systems authorized service facility. Contact Stanford Research Systems or an authorized representative before returning this product for repair.

Model numbers

This document is the User Manual for three models in the SG390 series of RF Signal Generators. The SG392, SG394 and SG396 provide front panel outputs of frequencies up to 2.025 GHz, 4.050 GHz and 6.075 GHz respectively.

Information in this document is subject to change without notice.

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Contents

Vector Modulation 45

Safety and Preparation for Use

Line Voltage

The instruments operate from a 90 to 132 V_{AC} or 175 to 264 V_{AC} power source having a line frequency between 47 and 63 Hz. Power consumption is less than 90 VA total. In standby mode, power is turned off to the main board. However, power is maintained at all times to the installed timebase. Units with the standard ovenized quartz oscillator or the optional rubidium timebase will consume less than 15 VA and 25 VA, respectively, in standby mode.

Power Entry Module

A power entry module, labeled AC POWER on the back panel of the instrument, provides connection to the power source and to a protective ground.

Power Cord

The unit is shipped with a detachable, three-wire power cord for connection to the power source and protective ground.

The exposed metal parts of the box are connected to the power ground to protect against electrical shock. Always use an outlet which has a properly connected protective ground. Consult with an electrician if necessary.

Grounding

BNC shields are connected to the chassis ground and the AC power source ground via the power cord. Do not apply any voltage to the shield.

Line Fuse

The line fuse is internal to the instrument and may not be serviced by the user.

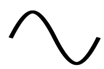
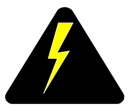
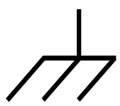
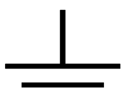
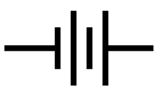
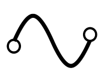
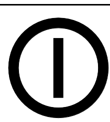
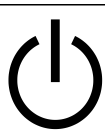
Operate Only with Covers in Place

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without all covers and panels in place.

Serviceable Parts

There are no user serviceable parts. Refer service to a qualified technician.

Symbols You May Find on SRS Products

Symbol	Description
	Alternating Current
	Caution – risk of electrical shock
	Frame or Chassis terminal
	Caution – refer to accompanying document
	Earth (ground) terminal
	Battery
	Fuse
	Power On
	Power Off
	Power Standby

Specifications

Frequency Setting (f_C)

Frequency ranges	
BNC output	DC to 62.5 MHz
Type N output	
SG392	950 kHz to 2.025 GHz
SG394	950 kHz to 4.050 GHz
SG396	950 kHz to 6.075 GHz
Frequency resolution	1 µHz at any frequency
Switching speed	<8 ms (to within 1 ppm)
Frequency error	$<(10^{-18}$ + timebase error$) \times f_C$
Frequency stability	$<1{:}10^{-11}$ (1 second Allan variance)

Front-Panel Type N Output (50 Ω load)

Frequency range	
SG392	950 kHz to 2.025 GHz
SG394	950 kHz to 4.050 GHz
SG396	950 kHz to 6.075 GHz
Output power	
SG392	+16.5 dBm to –110 dBm (1.5 V_{RMS} to 0.7 μV_{RMS})
SG394	+16.5 dBm (–3.50 dB/GHz above 3 GHz) to –110 dBm
SG396	+16.5 dBm (–3.25 dB/GHz above 4 GHz) to –110 dBm
Power resolution	0.01 dBm
Power accuracy	±1 dB (±2 dB above 4 GHz and above +5 dBm or below -100 dBm)
Output coupling	50 Ω, AC
User load	50 Ω
VSWR	<1.6
Reverse protection	30 V_{DC}, +25 dBm RF

Front-Panel BNC Output (50 Ω load)

Frequency range	DC to 62.5 MHz
Amplitude	
Full specs	1.00 to 0.001 V_{RMS} (+13 dBm to –47 dBm)
Derated specs	1.00 to 1.25 V_{RMS} (+14.96 dBm)
Offset	±1.50 V_{DC}
Maximum excursion	±1.817 V (amplitude + offset)
Amplitude resolution	<1 %
Amplitude accuracy	±5 %
Offset resolution	5 mV
Harmonics	<–40 dBc
Spurious	<–75 dBc
Output coupling	DC, 50 Ω ±2 %
User load	50 Ω
Reverse protection	±5 V_{DC}

Spectral Purity of the RF Output Referenced to 1 GHz [1]

Sub harmonics	None (No doublers are used.)
Harmonics	<–25 dBc with <+7 dBm on Type N output
Spurious	
Within 10 kHz of carrier	<–65 dBc
More than 10 kHz from carrier	<–75 dBc
Phase noise	
Offset from carrier	Phase Noise (typical)
10 Hz	–80 dBc/Hz
1 kHz	–102 dBc/Hz
20 kHz	
SG392 & SG394	–116 dBc/Hz
SG396	–114 dBc/Hz
1 MHz	
SG392 & SG394	–130 dBc/Hz
SG396	–124 dBc/Hz
Residual FM	1 Hz rms, typical, over 300 Hz to 3 kHz bandwidth
Residual AM	0.006 % rms, typical, over 300 Hz to 3 kHz bandwidth

(1) Spurs, phase noise and residual FM scale by 6 dB/octave to other carrier frequencies

Phase Setting of Front-Panel Outputs

Phase range	±360 °
Phase resolution	
DC to 100 MHz	0.01°
100 MHz to 1 GHz	0.1°
1 GHz to 8.1 GHz	1.0°

Internal Analog Modulation Source

Waveforms	Sine, ramp, saw, square, pulse, noise
Sine THD	–80 dBc (typical at 20 kHz)
Ramp linearity	<0.05 % (1 kHz)
Rate	
SG392 & SG394	
$f_C \leq$ 62.5 MHz	1 μHz to 500 kHz
$f_C >$ 62.5 MHz	1 μHz to 50 kHz
SG396	
$f_C \leq$ 93.75 MHz	1 μHz to 500 kHz
$f_C >$ 93.75 MHz	1 μHz to 50 kHz
Rate resolution	1 μHz
Rate error	<1:2^{31} + timebase error
Noise function	White Gaussian noise, RMS = DEV / 5
Noise bandwidth	1 μHz < ENBW < 50 kHz
Pulse generator period	1 μs to 10 s
Pulse generator width	100 ns to 9999.9999 ms
Pulse timing resolution	5 ns
Pulse noise function	PRBS length: $2^N – 1$with $5 \leq N \leq 32$ Bit period (100 + n·5) ns, 100 ns to 10 s in 5 ns steps

Analog Modulation Waveform Output

Output impedance	50 Ω (for reverse termination)
User load	Unterminated 50 Ω coax
AM, FM, ΦM	±1 V for ± full deviation
Pulse/Blank	"Low" = 0 V, "High" = 3.3 V_{DC}
Connector	Rear-panel BNC

External Analog Modulation Input

Modes	AM, FM, ΦM, Pulse and Blank
Unmodulated level	0 V input for unmodulated carrier
AM, FM, ΦM	±1 V input for ± full deviation
Modulation bandwidth	>100 kHz
Modulation distortion	<–60 dB
Input impedance	100 kΩ
Input Coupling	AC (4 Hz high pass) or DC
Input offset	<500 µV
Pulse/Blank threshold	+1 V_{DC}
Connector	Rear-panel BNC

Analog Frequency Modulation

Frequency deviation	
Minimum	0.1 Hz
Maximum	
SG392 & SG394	
$f_C \leq 62.5$ MHz:	Smaller of f_C or (64 MHz – f_C)
62.5 MHz < $f_C \leq$ 126.5625 MHz	1 MHz
126.5625 MHz < $f_C \leq$ 253.1250 MHz	2 MHz
253.1250 MHz < $f_C \leq$ 506.25 MHz	4 MHz
506.25 MHz < $f_C \leq$ 1.0125 GHz	8 MHz
1.0125 GHz < $f_C \leq$ 2.025 GHz	16 MHz
2.025 GHz < $f_C \leq$ 4.050 GHz (SG394)	32 MHz
SG396	
$f_C \leq 93.75$ MHz:	Smaller of f_C or (96 MHz – f_C)
93.75 MHz < $f_C \leq$ 189.84375 MHz	1 MHz
189.84375 MHz < $f_C \leq$ 379.6875 MHz	2 MHz
379.6875 MHz < $f_C \leq$ 759.375 MHz	4 MHz
759.375 MHz < $f_C \leq$ 1.51875 GHz	8 MHz
1.51875 GHz < $f_C \leq$ 3.0375 GHz	16 MHz
3.0375 GHz < $f_C \leq$ 6.075 GHz	32 MHz

Analog Frequency Modulation (continued)

Deviation resolution	0.1 Hz
Deviation accuracy	
SG392 & SG394	
$f_C \leq 62.5$ MHz	<0.1 %
$f_C > 62.5$ MHz	<3 %
SG396	
$f_C \leq 93.75$ MHz	<0.1 %
fc > 93.75 MHz	<3 %
Modulation source	Internal or external
Modulation distortion	<–60 dB (f_C = 100 MHz, f_M = 1 kHz, f_D = 1 kHz)
Ext FM carrier offset	<1:1000 of deviation
Modulation bandwidth	
SG392 & SG394	
$f_C \leq 62.5$ MHz	500 kHz
$f_C > 62.5$ MHZ	100 kHz
SG396	
$f_C \leq 93.75$ MHz	500 kHz
$f_C > 93.75$ MHZ	100 kHz

Phase Continuous Frequency Sweeps

Frequency span	0.1 Hz to entire sweep range
Sweep ranges	
SG392 & SG394	
	DC to 64 MHz
	59.375 to 128.125 MHz
	118.75 to 256.25 MHz
	237.5 to 512.5 MHz
	475 to 1025 MHz
	950 to 2050 MHz
	1900 to 4100 MHz (SG394)
SG396	
	DC to 96 MHz
	89.0625 to 192.1875 MHz
	178.125 to 384.375 MHz
	356.25 to 768.75 MHz
	712.5 to 1537.5 MHz
	1425 to 3075 MHz
	2850 to 6150 MHz
Deviation resolution	0.1 Hz
Sweep source	Internal or external
Sweep distortion	<0.1 Hz + (deviation / 1000)
Sweep offset	<1:1000 of deviation
Sweep function	Triangle, ramps, or sine up to 120 Hz

Analog Phase Modulation

Deviation	0 to 360°
Deviation resolution	
DC < $f_C \le 100$ MHz	0.01°
100 MHz < $f_C \le 1$ GHz	0.1°
$f_C > 1$ GHz	1.0°
Deviation accuracy	
SG392 & SG394	
$f_C \le 62.5$ MHz	<0.1 %
$f_C > 62.5$ MHZ	<3 %
SG396	
$f_C \le 93.75$ MHz	<0.1 %
$f_C > 93.75$ MHZ	<3 %
Modulation source	Internal or external
Modulation distortion	<–60 dB ($f_C = 100$ MHz, $f_M = 1$ kHz, $\Phi_D = 50°$)
Modulation bandwidth	
SG392 & SG394	
$f_C \le 62.5$ MHz	500 kHz
$f_C > 62.5$ MHz	100 kHz
SG396	
$f_C \le 93.75$ MHz	500 kHz
$f_C > 93.75$ MHz	100 kHz

Analog Amplitude Modulation

Range	0 to 100 % (Decreases above +7 dBm output)
Resolution	0.1 %
Modulation source	Internal or external
Modulation distortion ($f_M = 1$ kHz, Depth = 50%)	
$f_C \le 62.5$ MHz, BNC output	<1 %
$f_C > 62.5$ MHz, Type N output	<3 % typical
Modulation bandwidth	>100 kHz

Pulse/Blank Modulation

Pulse mode	Logic "high" turns BNC and RF on
Blank mode	Logic "high" turns BNC and RF off
On/Off ratio	
BNC output	70 dB
Type N output	
f_C <1 GHz	57 dB
1 GHz $\le f_C <$ 4 GHz	40 dB
$f_C \ge$ 4GHz	35 dB
Pulse feed-through	10 % of carrier for 20 ns at turn-on (typical)
Turn on/off delay	60 ns
RF rise/fall time	20 ns
Modulation source	Internal or external pulse

Dual Baseband Generator for Vector I/Q Modulation

Symbol source	User symbol data, PRBS, or 16-bit settable pattern
PRBS length	$2^N - 1$, with $5 \le N \le 32$ (31 to about 4.3×10^9 symbols)
User symbols	Up to 16 Mbits
Symbol rate	1 Hz to 6 MHz (12 MHz for VSB) with μHz resolution
Symbol length	1 to 9 bits (maps to constellation) or two 16-bit values for I & Q
Symbol mapping	Default or user defined constellation
Digital filters	Nyquist, root Nyquist, Gaussian, rectangular, triangle, sinc, linearized Gaussian, C4FM, user FIR
Filter length	24 symbols
DAC data source	Computed in real time from symbols, constellation & filter
DAC data format	Dual 14-bit at 125 Msps
Reconstruction filter	10 MHz, 3rd order , Bessel, low pass filter
Vector modulation	PSK, QAM, FSK, CPM, MSK, ASK, VSB
PSK derivatives	BPSK, QPSK, OQPSK, DQPSK, π/4DQPSK, 8 PSK 16 PSK, 3π/8 8 PSK
QAM derivatives	4, 16, 32, 64, and 256
FSK derivatives	1-bit to 4-bit, with deviations from 0 to 6 MHz
ASK derivatives	1-bit to 4-bit
CPM derivatives	1-bit to 4-bit, with modulation indices from 0 to 1.0
VSB derivatives	8 and 16 (at rates up to 12 Msps)
Preset Modes	GSM, GSM-EDGE, W-CDMA, APCO-25, DECT, NADC, PDC, TETRA, ATSC-DTV, and audio clip for analog AM & FM
Rear event markers	Symbol clock, data frame, TDMA, and user-defined
Additive noise	White, Gaussian, –70 dBc to –10 dBc, bandlimited by selected digital filter

Typical EVM or FSK Errors (rms at 0 dBm output)

TETRA (π/4 DQPSK, 18.0 ksps, 420 MHz)	0.76 %
NADC (π/4 DQPSK, 24.3 ksps, 875 MHz)	0.33 %
APCO-25 (FSK4-C4FM, 4.8 ksps, 850 MHz)	0.46 %
DECT (FSK2, 1.152 Mbps, 1.925 GHz)	1.5 %
GSM (GMSK, 270.833 ksps, 935 MHz)	0.30 %
GSM (GMSK, 270.833 ksps, 1.932 GHz)	0.60 %
EDGE (3π/8 8PSK, 270.833 ksps, 935 MHz)	0.30 %
EDGE (3π/8 8PSK, 270.833 ksps, 1.932 GHz)	0.50 %
W-CDMA (QPSK, 3.840 Mcps, 1.850 GHz)	1.7%
QAM256 (6 Msps, 2.450 GHz)	1.1%
QAM32 (6 Msps 5.800 GHz)	1.6%
ATSC-DTV (8VSB, 10.762 Msps, 695 MHz)	2.2%

External I/Q Modulation

Modulated output	Front-panel Type N only (+10 dBm max)
Frequency range	Carrier frequencies above 400 MHz
I/Q inputs	50 Ω, ±0.5 V, (rear BNCs)
I or Q input offset	<500 µV
I/Q full scale	$(I^2 + Q^2)^{1/2} = 0.5$ V
Carrier suppression	>40 dBc (>35 dBc above 4 GHz)
Modulation bandwidth	300 MHz RF bandwidth

Timebase Input

Frequency	10 MHz, ±2 ppm
Amplitude	0.5 to 4 V_{PP} (–2 dBm to +16 dBm)
Input impedance	50 Ω, AC coupled

Timebase Output

Frequency	10 MHz, sine
Source	50 Ω, DC transformer coupled
Amplitude	1.75 V_{PP} ±10 % (8.8 ± 1 dBm)

Standard OCXO Timebase

Oscillator type	Oven controlled, 3rd OT, SC-cut crystal
Stability	<0.002 ppm (0 to 45°C)
Aging	<0.05 ppm/year

Rubidium Timebase (Option 4)

Oscillator type	Oven controlled, 3rd OT, SC-cut crystal
Physics package	Rubidium vapor frequency discriminator
Stability	<0.0001 ppm (0 to 45°C)
Aging	<0.001 ppm/year

Computer Interfaces (all are standard)

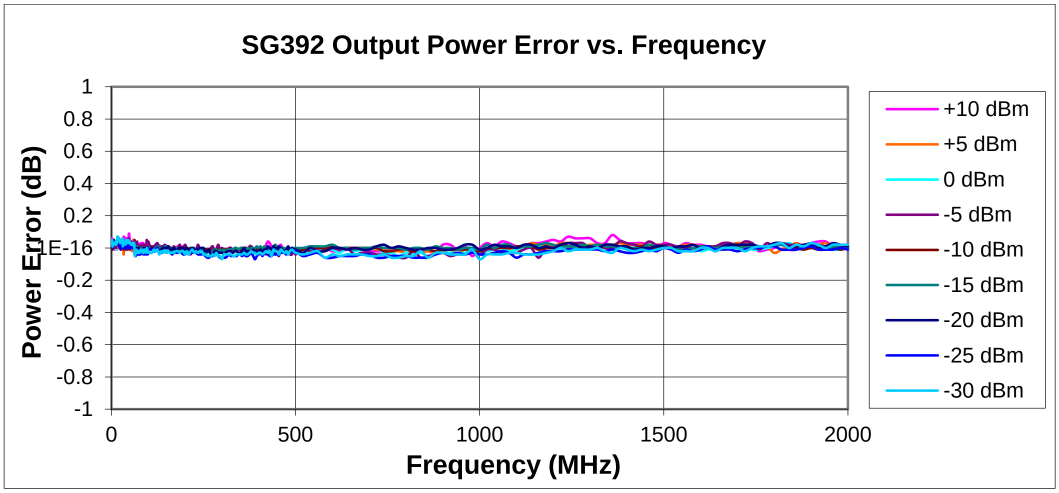
Ethernet (LAN)	10/100 Base-T. TCP/IP & DHCP default.
GPIB	IEEE-488.2
RS-232	4.8k-115.2k baud, RTS/CTS flow

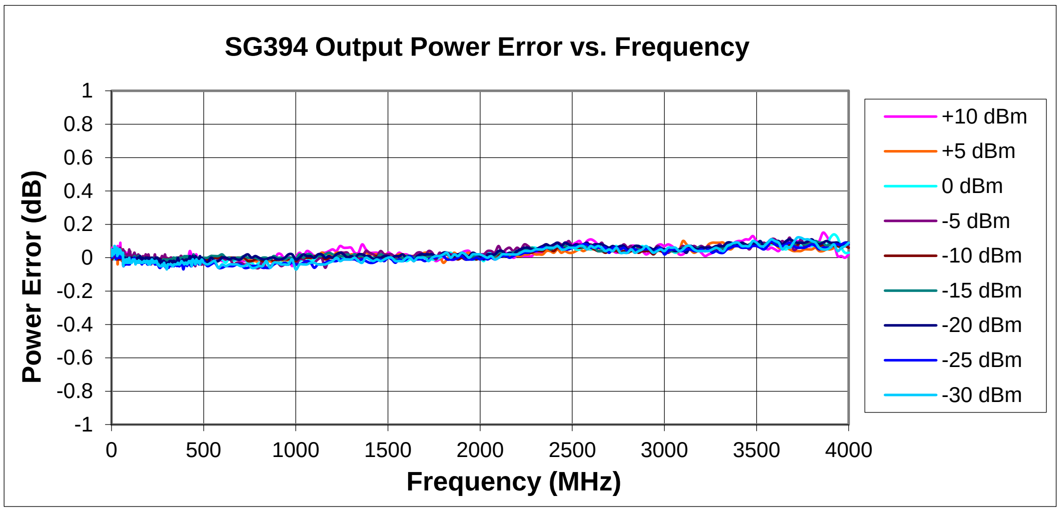
General

Line power	<90 W, 90 to 264 V_{AC}, 47 to 63 Hz with PFC
EMI Compliance	FCC Part 15 (Class B), CISPR-22 (Class B)
Dimensions	8.5” × 3.5” × 13” (W × H × D)
Weight	<10 lbs
Warranty	One year on parts and labor

Typical Operating Performance

Power Level Accuracy





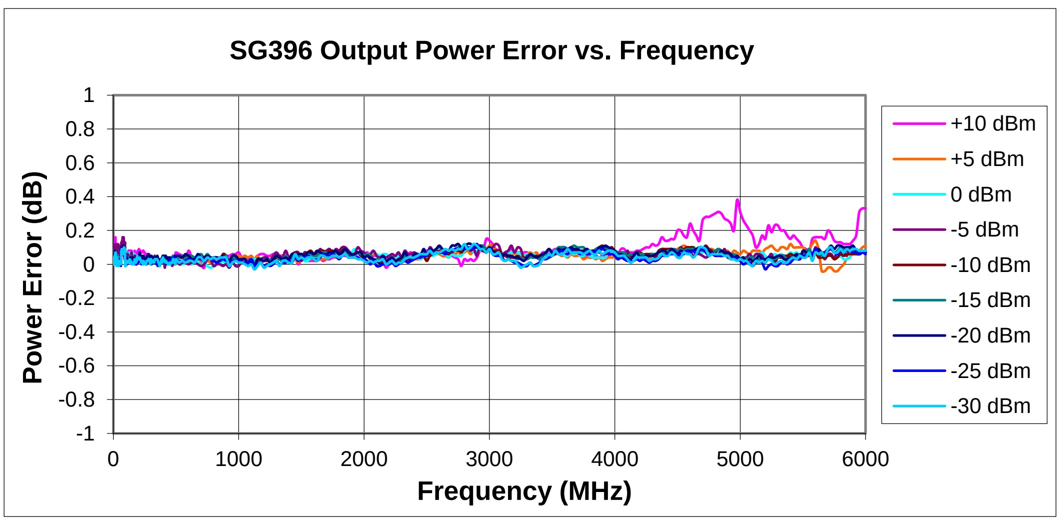
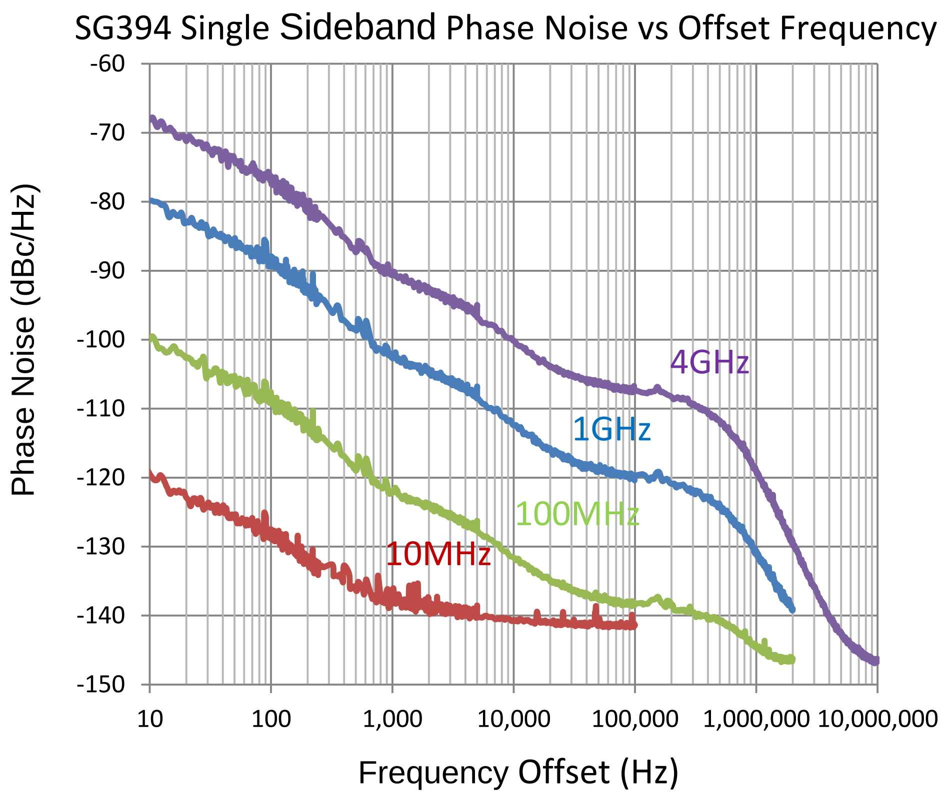


Figure 1: Typical power level accuracy for SG392, SG394, and SG396

Single Sideband Phase Noise



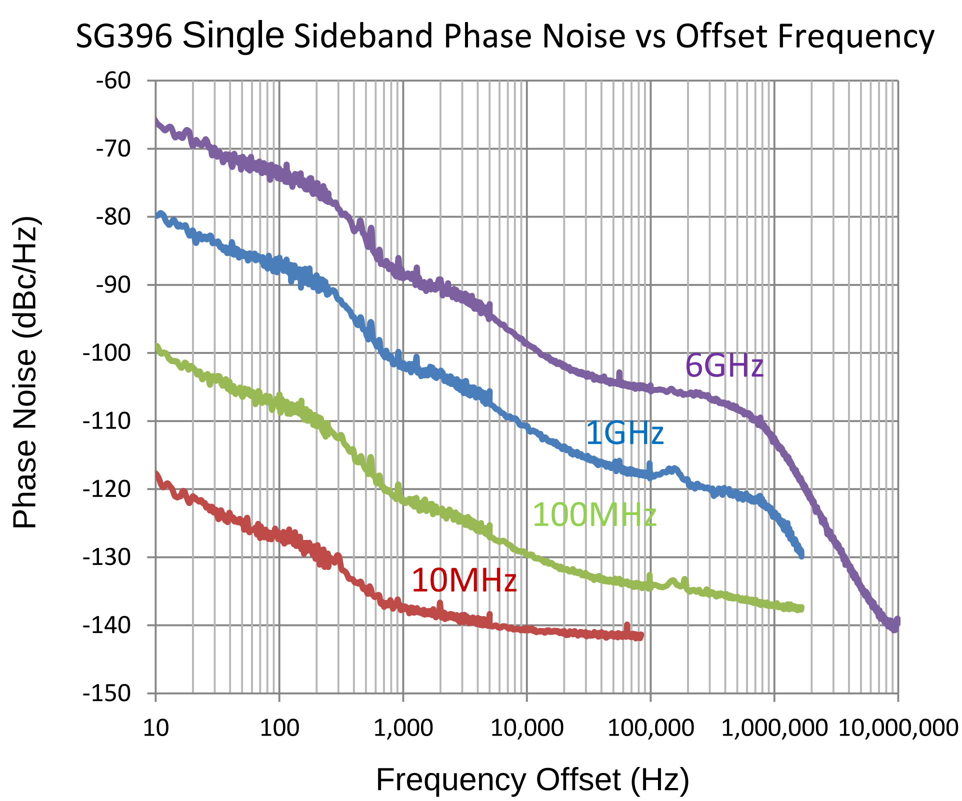
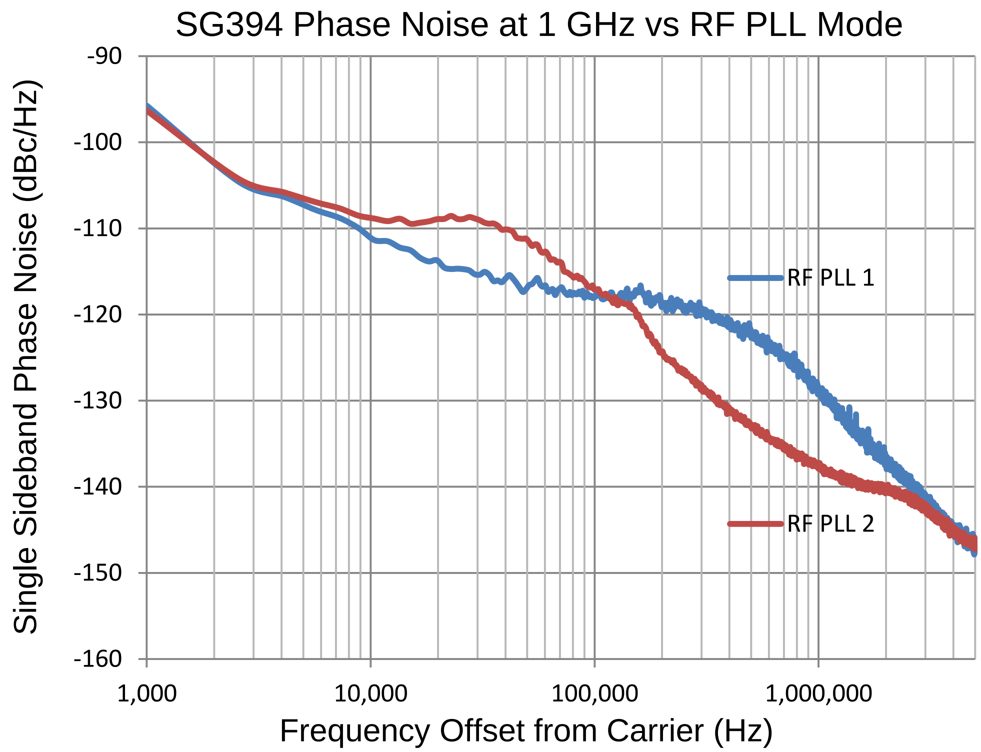


Figure 2: Typical single sideband phase noise performance for SG394 and SG396

Single Sideband Phase Noise vs RF PLL Mode



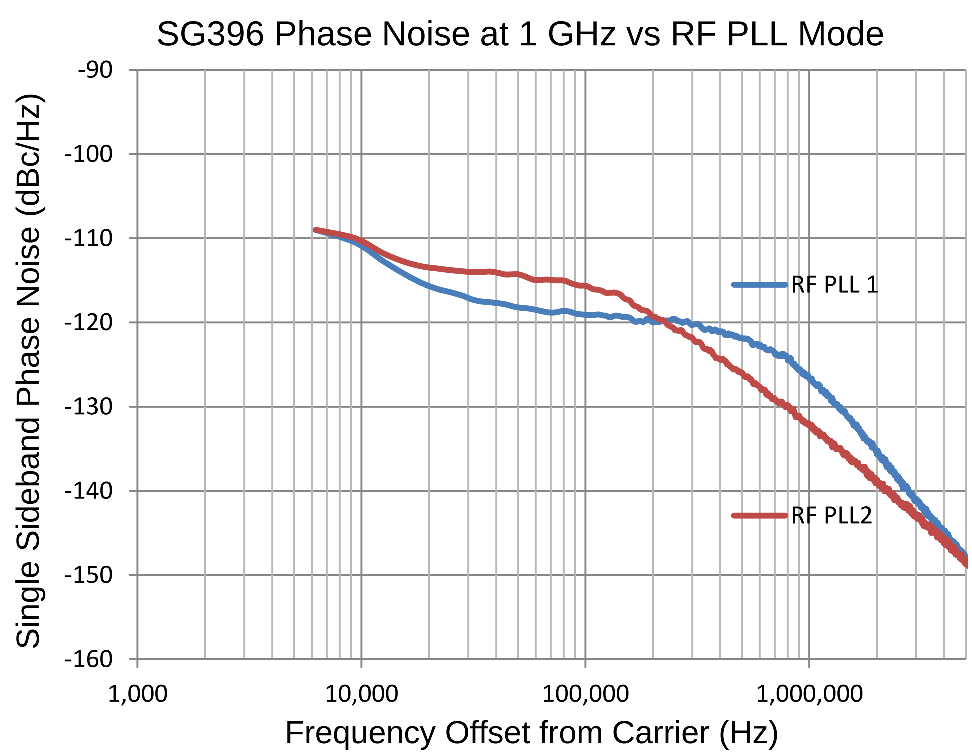


Figure 3: Phase noise vs RF PLL mode for SG394 and SG396. PLL 1 is the default. Mode is selected via the front panel CAL menu (see page 22).

Spectral Purity

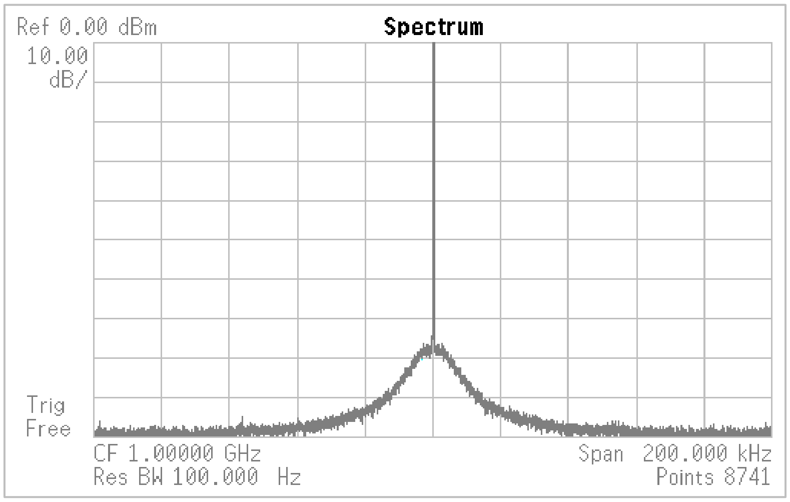


Figure 4: Typical spectra of the SG394 for a 0 dBm signal at 1 GHz. The spectrum analyzer is configured with a 200 kHz span and a 100 Hz resolution bandwidth. The noise floor of the spectrum analyzer dominates over most of the 200 kHz span.

Analog AM Modulation

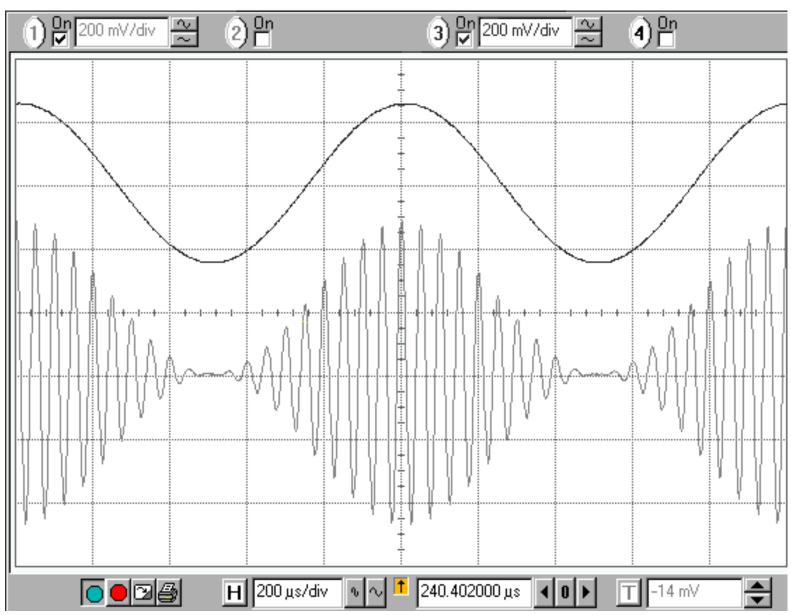


Figure 5: Scope traces for the rear panel modulation output (top) and the front panel BNC output (bottom). The SG394 was configured for sine wave AM modulation of a 20 kHz, 1 V_{pp} carrier at a modulation rate of 1 kHz and 100 % AM depth.

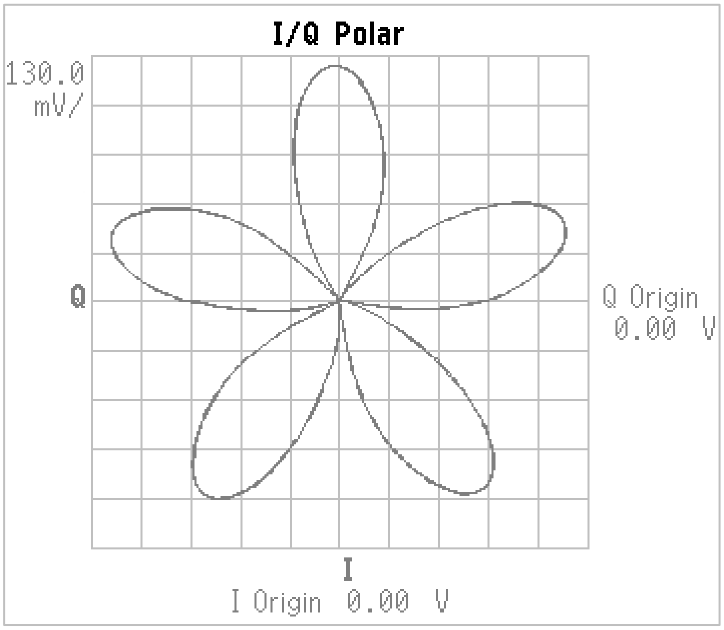


Figure 6: I/Q demodulation of a 1 GHz, 0 dBm carrier configured with 100 % sine wave analog AM modulation at 5 kHz. The pattern shown above occurs when the center frequency of the spectrum analyzer is offset by 1 kHz. The modulation rate is five times the offset frequency, thus creating five lobes in the demodulated I/Q plane. The symmetry of the lobes indicates that there is no residual phase distortion (AM to ΦM conversion) in the amplitude modulator. The narrow line of the trajectory is indicative of low phase and amplitude noise.

Analog FM Modulation

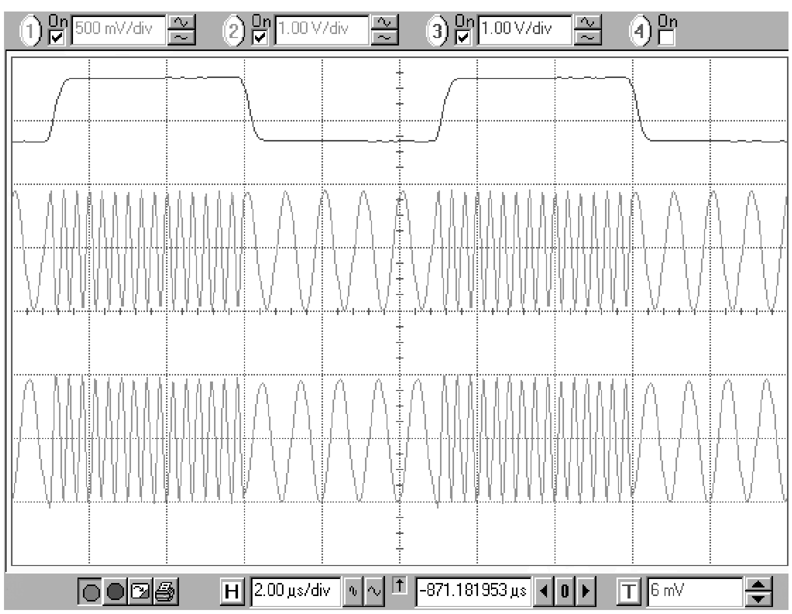


Figure 7: Scope traces for the rear panel modulation output (top), the front panel BNC output (middle), and the front panel Type N output (bottom). The SG394 was configured for analog, square wave, frequency modulation (FSK) of a 2 MHz carrier at a modulation rate of 100 kHz and a frequency deviation of 1 MHz. The amplitude was configured to be 1 V_{pp} for the BNC output and 2 V_{pp} for the Type N output.

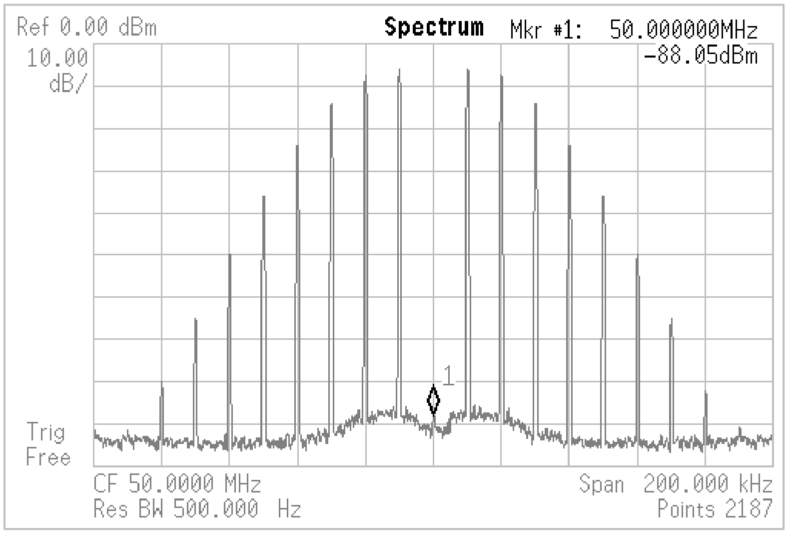


Figure 8: Spectra for a 50 MHz, 0 dBm carrier configured for sine wave, analog FM modulation at 10 kHz and a frequency deviation of 24.0477 kHz. This corresponds to a modulation index of β = 2.40477. For FM modulation, the carrier amplitude is proportional to the Bessel function $J_0(\beta)$ which has its first zero at 2.40477, thus the suppressed carrier.

Pulse Modulation

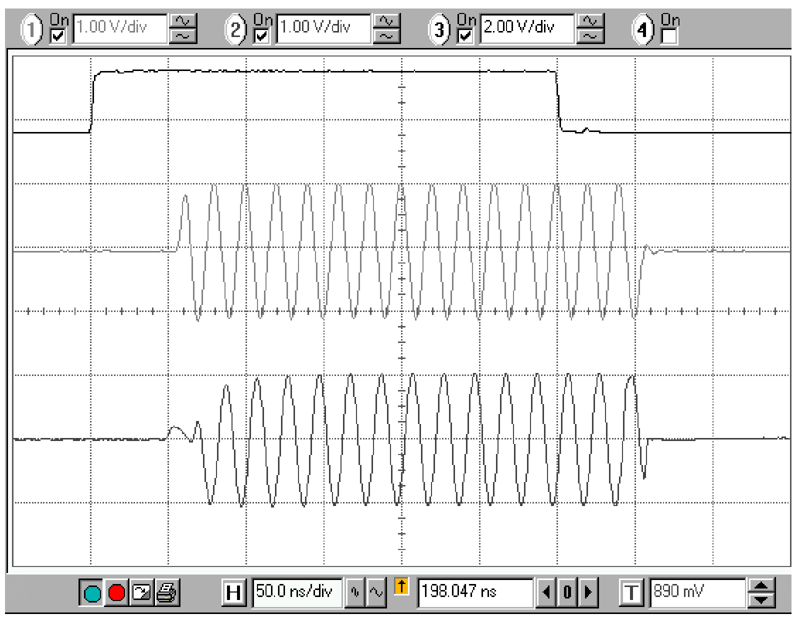


Figure 9: Scope traces for the rear panel modulation output (top), the front panel BNC output (middle), and the front panel Type N output (bottom). The SG394 was configured for 300 ns pulse modulation of a 50 MHz carrier at 1 MHz (1 µs period). The BNC and Type N outputs were both configured for 2 V_{pp} signals. There are delays of 50 ns in the gating circuitry as shown.

External I/Q Bandwidth

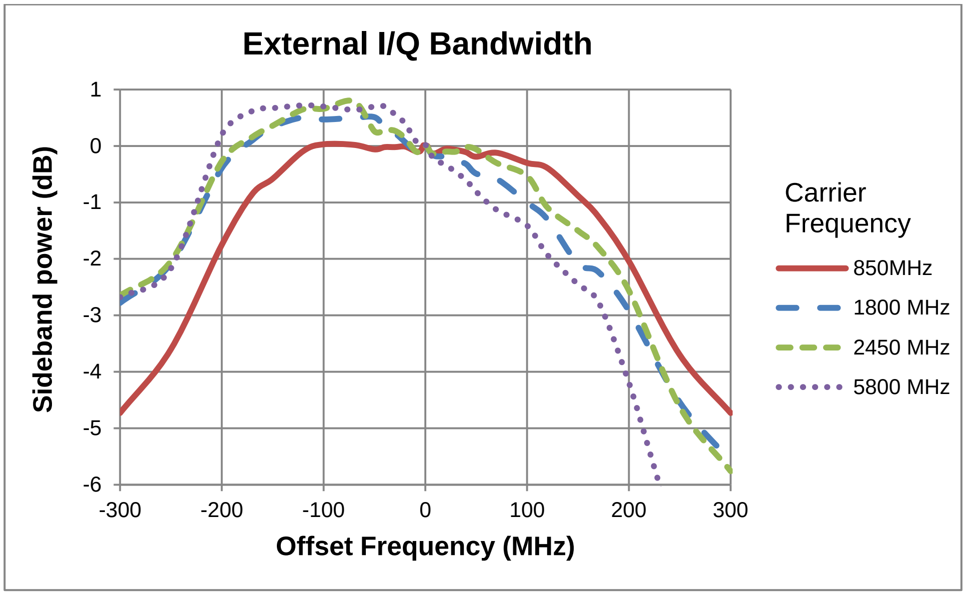


Figure 10: External I/Q modulation bandwidth characteristic. For low frequency carriers, such as 850 MHz, the modulation characteristics are very flat and symmetric, with a –1 dB RF bandwidth of over 300 MHz. The internal baseband generator has only a 10 MHz bandwidth and so there is no need to compensate for these characteristics. For high bandwidth external I/Q modulation, however, compensatory digital filters (predistortion) should be used to optimize EVMs at high carrier frequencies.

GSM

Constellation

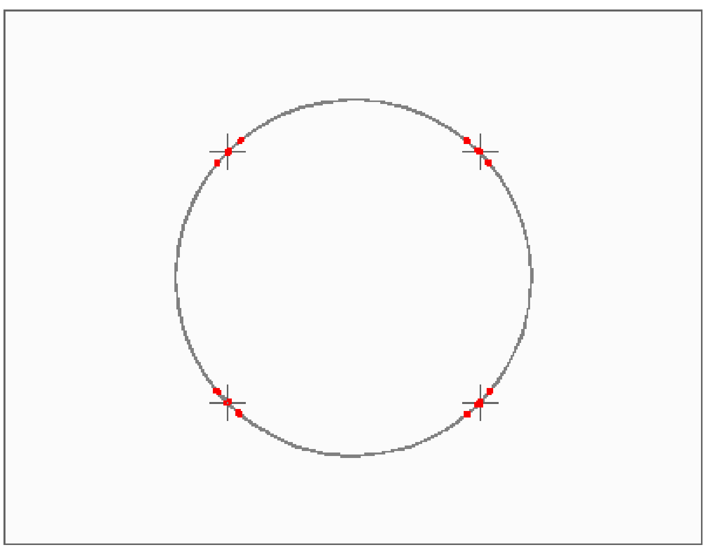


Figure 11: I/Q demodulation of the GSM waveform generated by the SG396 using the GSM modulation preset at 935.2MHz. GSM is a constant envelope modulation as indicated by the circular path of the demodulated I/Q. The nearest neighbor intersymbol interference (ISI) of the waveform is also evident with the presence of the two symbol dots on either side of the main symbol dot for each allowed phase.

Eye Diagram

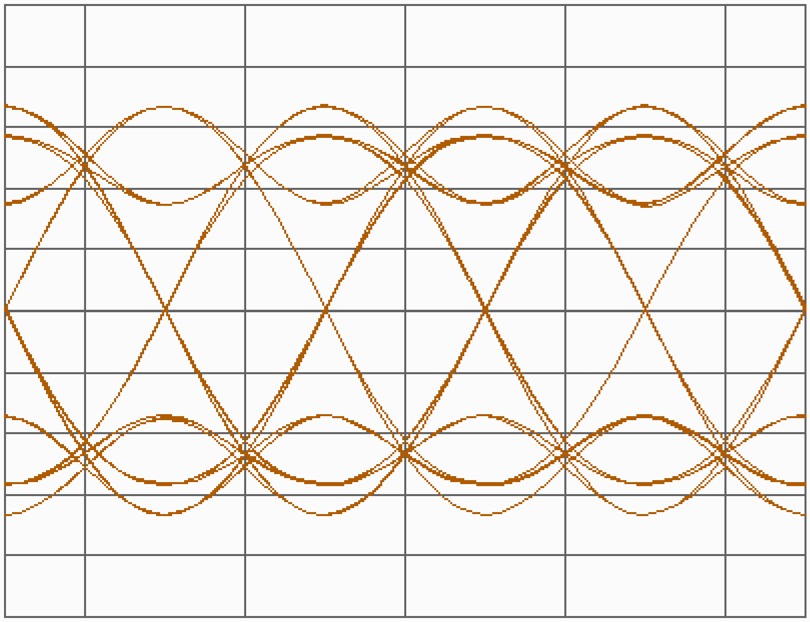


Figure 12: I eye diagram for the demodulated GSM waveform as generated by the SG396 using the GSM modulation preset at 935.2MHz. The nearest neighbor intersymbol interference (ISI) of the Gaussian filter is evident with 3 separate crossovers at each symbol boundary location.

Power Mask

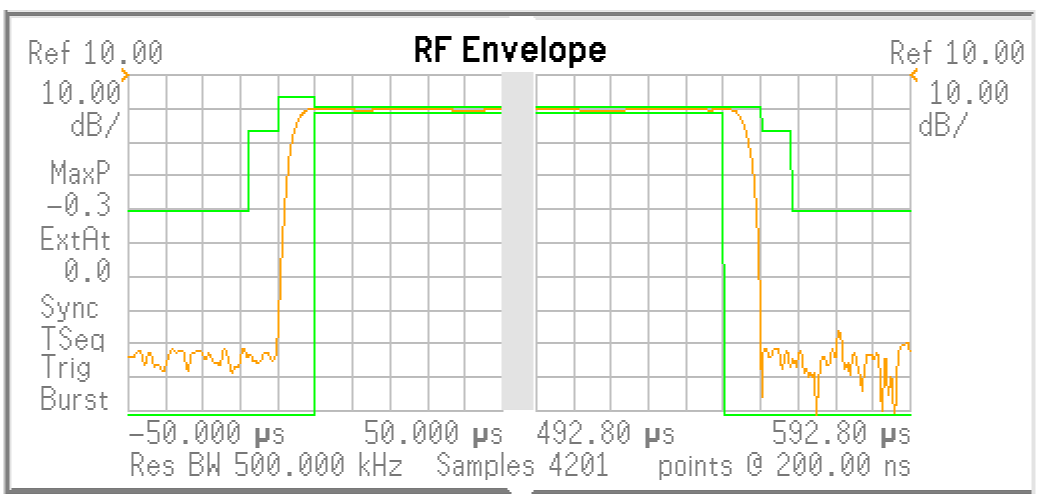


Figure 13: RF Power vs time for the demodulated GSM waveform as generated by the SG396 using the GSM modulation preset at 935.2MHz. GSM uses a TDMA access protocol with a 4.62 ms frame divided into eight TDMA slots lasting 577 μs. Within a TDMA time slot, 148 symbols are transmitted at a rate of 270.833 kHz. Shown above, is the RF power vs time at the beginning and end of the TDMA time slot.

GSM EDGE

Constellation

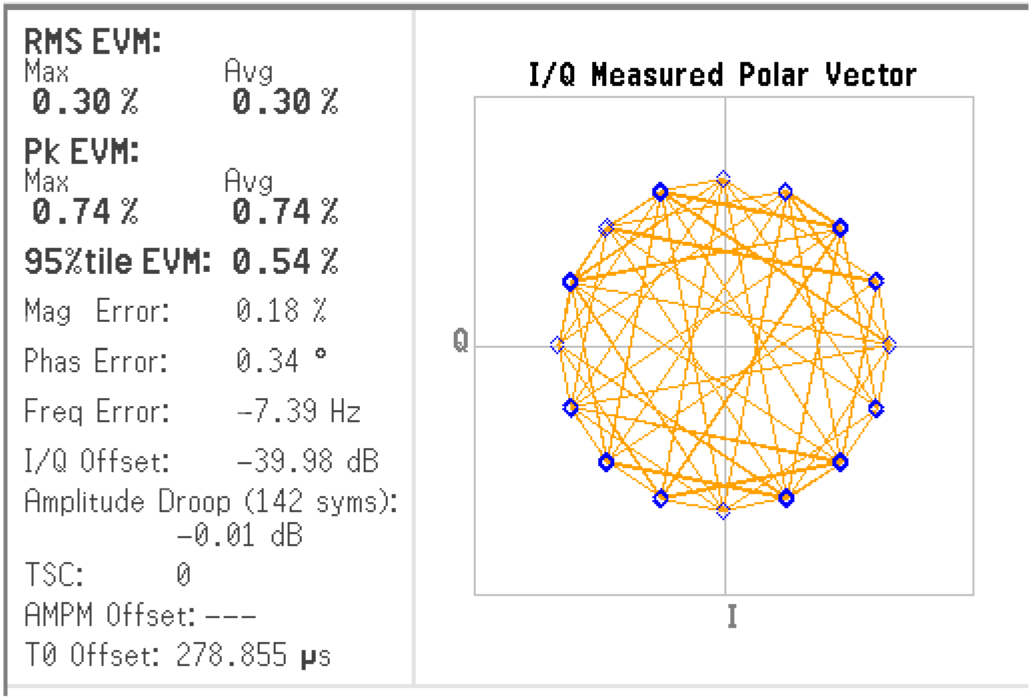


Figure 14: I/Q demodulation and performance statistics of GSM EDGE waveform as generated by SG396 using the GSM EDGE modulation preset at 935.2 MHz.

Power Mask

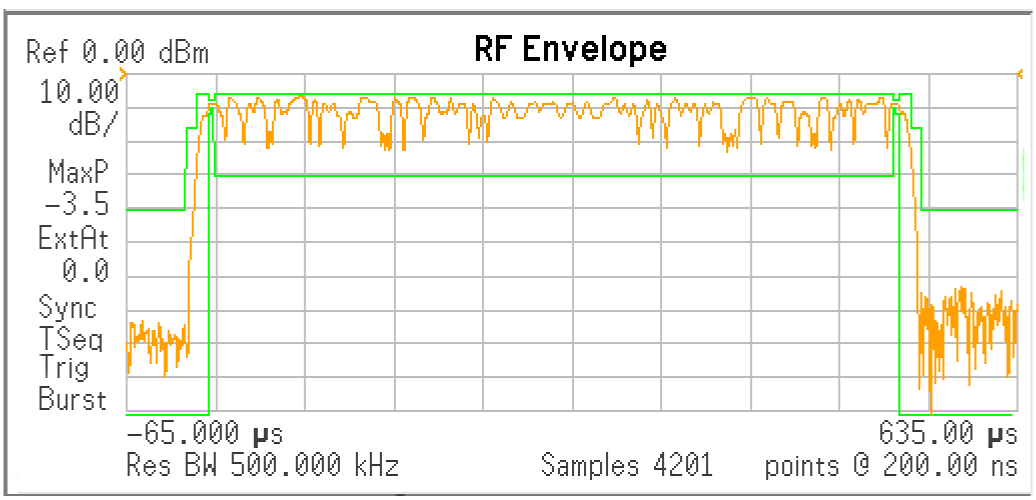


Figure 15: RF Power vs time for the demodulated GSM EDGE waveform as generated by the SG396 using the GSM EDGE modulation preset at 935.2MHz. GSM EDGE uses a TDMA access protocol with a 4.62 ms frame divided into eight TDMA slots lasting 577 μs. Within a TDMA time slot, 148 symbols are transmitted at a rate of 270.833 kHz. Shown above, is the RF power vs time for the RF burst during the TDMA time slot.

TETRA

Constellation

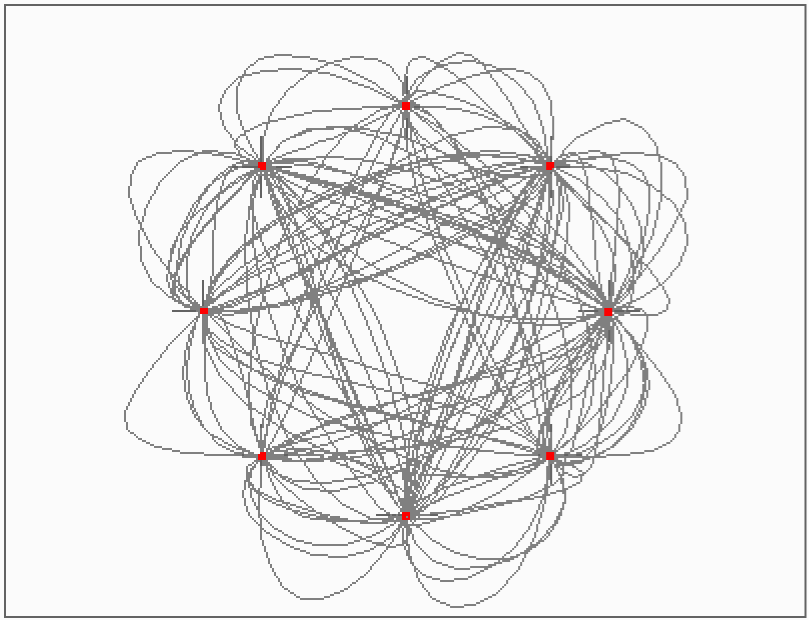


Figure 16: I/Q demodulation of the TETRA waveform as generated by the SG396 using the TETRA modulation preset at 420 MHz. TETRA uses π/4 DQPSK with a data rate of 18 ksps and a root Nyquist pulse shaping filter with α = 0.35. The 2-bit symbols are mapped into a 4 symbol constellation that is rotated by π/4 after each symbol, which is why the constellation appears to contain 8 symbols.

Eye Diagram

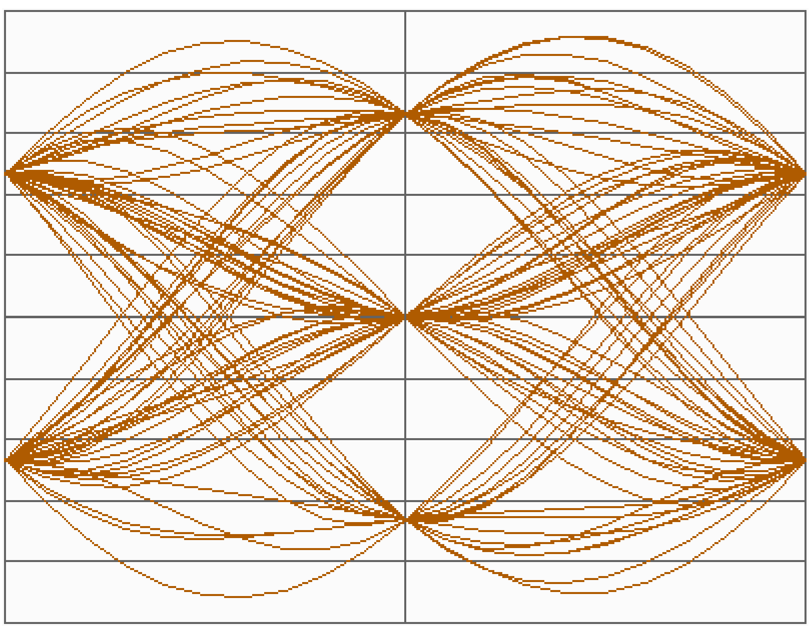


Figure 17: I/Q demodulation of the TETRA waveform as generated by the SG396 using the TETRA modulation preset at 420 MHz. The measured rms EVM was 0.7 %.

APCO 25

Constellation

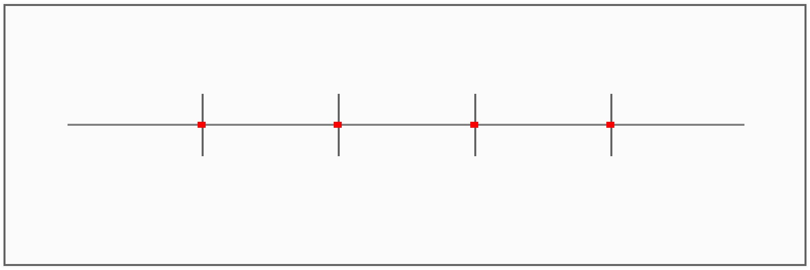


Figure 18: Demodulation of the APCO 25 waveform as generated by the SG396 using the APCO 25 modulation preset at 850 MHz. APCO 25 uses a special form of 4 FSK modulation named C4FM with a symbol rate of 4800 Hz and a frequency deviation of 1800 Hz. The special pulse shaping filter required by C4FM is included as part of the preset.

Eye Diagram

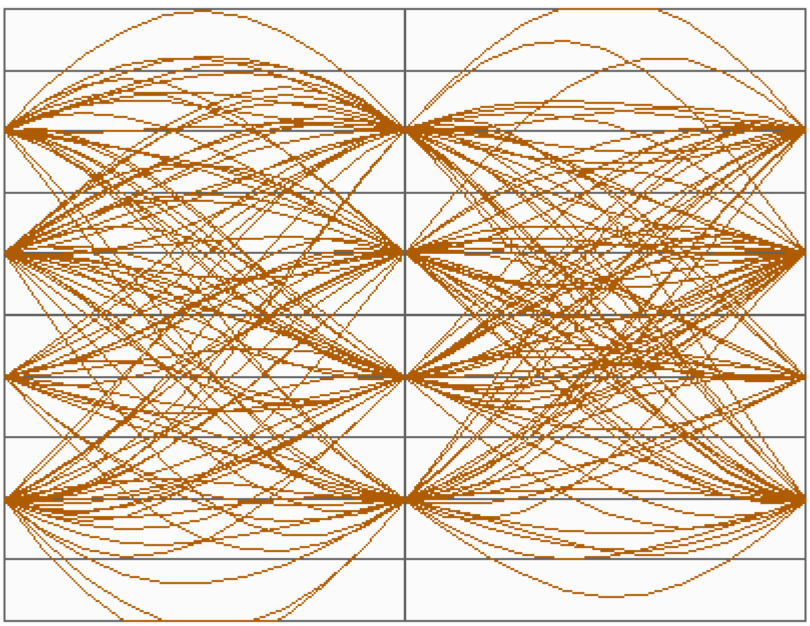


Figure 19: Demodulation of the APCO 25 waveform as generated by the SG396 using the APCO 25 modulation preset at 850 MHz. The measured rms FSK frequency error was 0.5 %.

QAM 16

Constellation

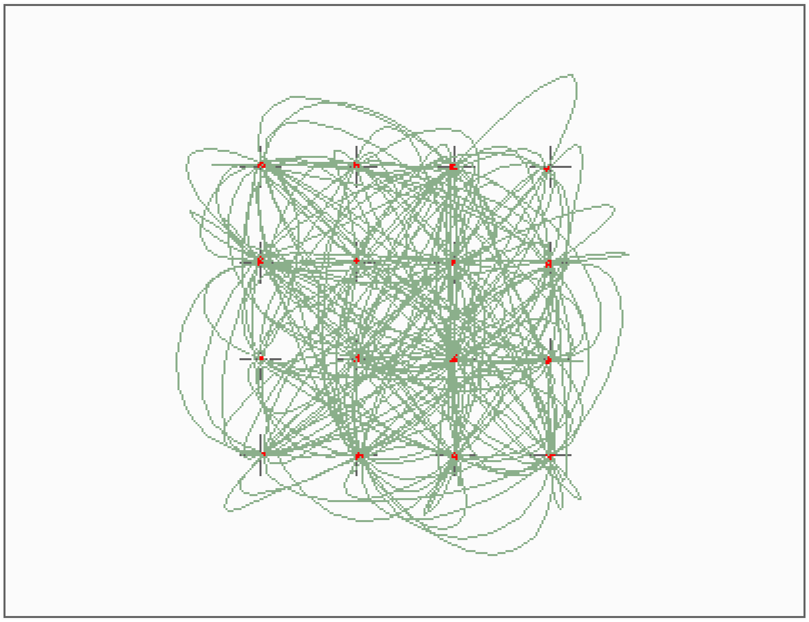


Figure 20: Demodulation of QAM 16 as generated by the SG396 at 2.45 GHz. The waveform consisted of PRBS 32 symbols modulated at 6 Msps with a root Nyquist pulse shaping filter of α = 0.2.

Eye Diagram

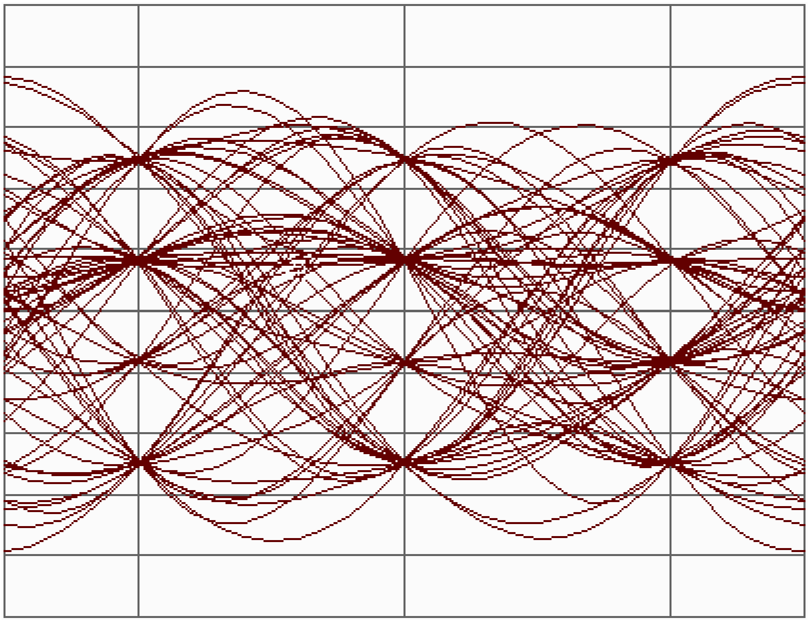


Figure 21: Demodulation of the I channel of QAM 16 as generated by the SG396 at 2.45 GHz. The waveform consisted of PRBS 32 symbols modulated at 6 Msps with a root Nyquist pulse shaping filter of α = 0.2. The measured rms EVM was 1.2 %.

QAM 256

Constellation

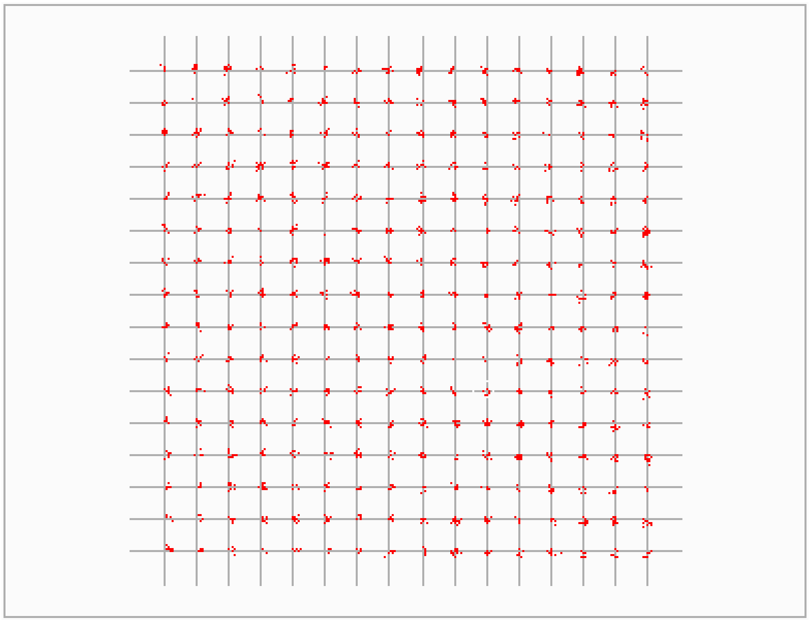


Figure 22: Demodulation of QAM 256 as generated by the SG396 at 2.45 GHz. The waveform consisted of PRBS 32 symbols modulated at 6 Msps with a root Nyquist pulse shaping filter of α = 0.2. The measured rms EVM was 1.0 %

ATSC-DTV (8 VSB)

Spectrum

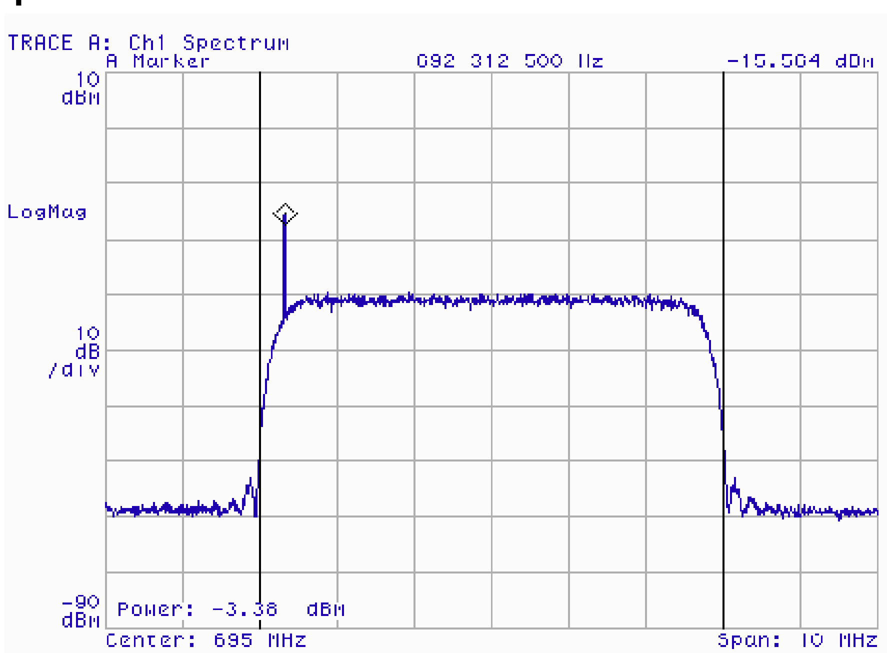


Figure 23: Spectrum for ATSC-DTV waveform as generated by the SG396 using the ATSC-DTV modulation preset at 695 MHz (channel 51). The signal is shown with a 10 kHz RBW. It clearly shows the 6 MHz bandwidth of the signal with the pilot tone at 692.31 MHz. The noise floor outside the 6MHz signal is that of the spectrum analyzer.

Constellation

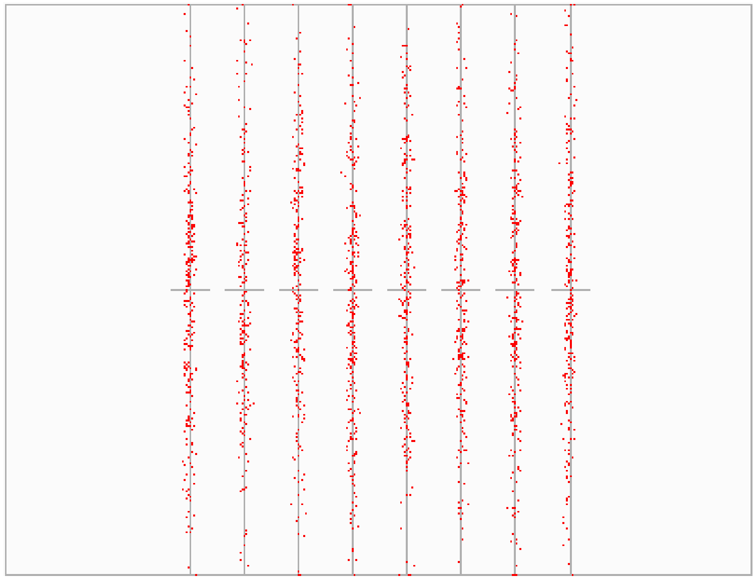


Figure 24: Demodulation of the ATSC-DTV waveform as generated by the SG396 using the ATSC-DTV modulation preset at 695 MHz (channel 51). The modulation is 8 VSB with PRBS 32 symbols at 10.762 Msps and a root Nyquist pulse shaping filter of α = 0.115. For 8 VSB, only the I channel is well defined at the symbol clock boundary. The Q channel spreads vertically as required to cancel the lower sideband. The measured rms EVM for the modulation was 2.3 %.

Event Markers and TDMA

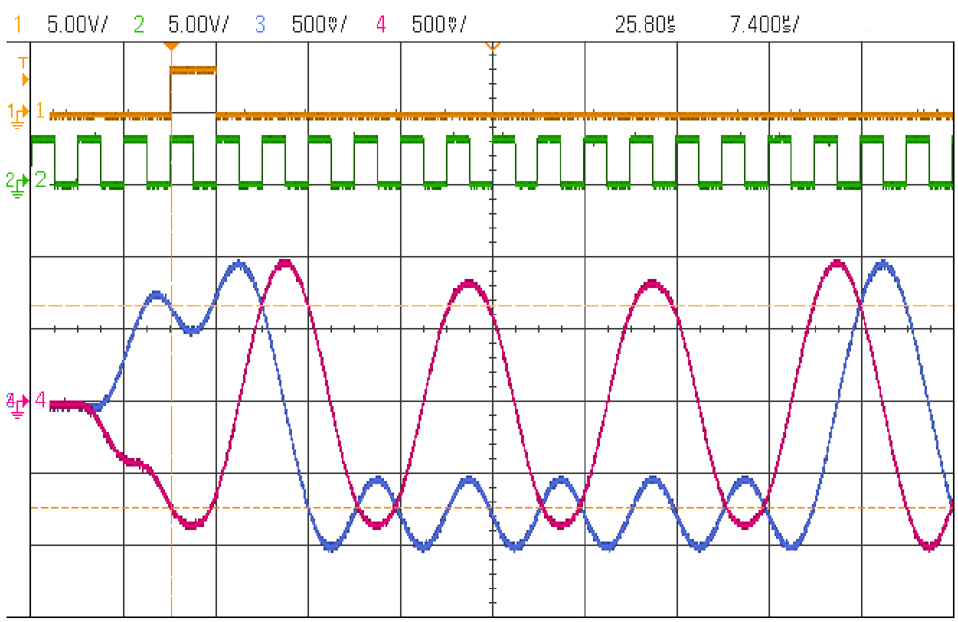


Figure 25: Oscilloscope trace of the rear panel outputs of the SG396 including frame sync marker (chn 1), symbol clock (chn 2), I output (chn 3), and Q output (chn 4) for the GSM waveform as generated by the SG396 using GSM modulation preset. The frame sync marker identifies the start of the GSM frame. Not shown, is the TDMA frame marker which goes high 2 symbols before the frame sync causing the RF power to ramp up. Note that the phase of the I/Q outputs are well defined, crossing the cursors, at the rising edges of the symbol clock.

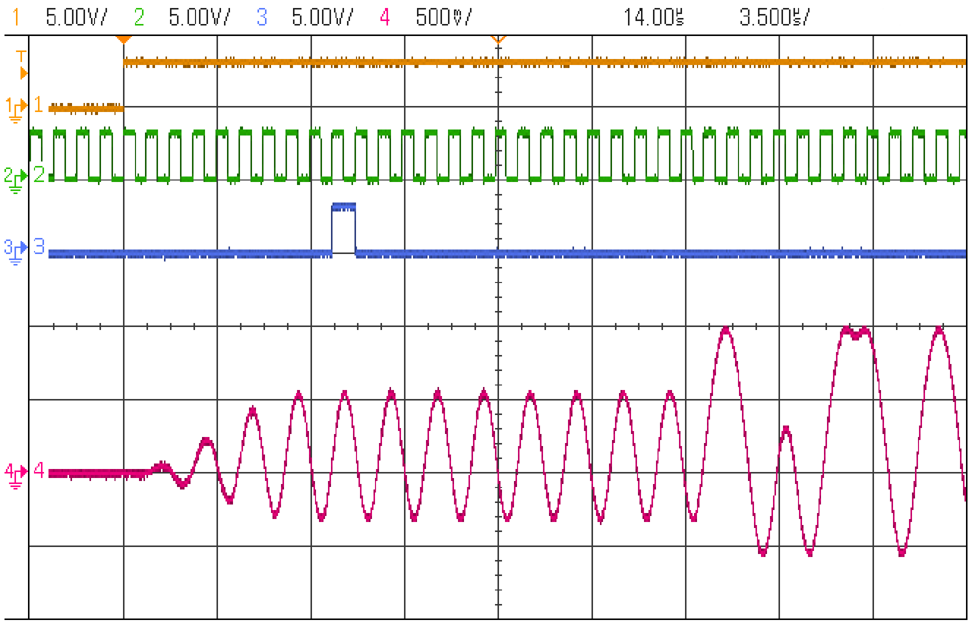


Figure 26: Oscilloscope trace of the rear panel outputs of the SG396 including the TDMA frame marker (chn 1), symbol clock (chn 2), frame sync marker (chn 3), and I output (chn 4) for the DECT waveform as generated by the SG396 using the DECT modulation preset. The RF power ramps up over 8 symbol periods after the TDMA frame marker goes high. The frame sync identifies the start of the DECT frame. The first 16 bits are a fixed preamble, which is followed by a random data pattern.

Quick Start Instructions

This is intended to help the first time users get started with the RF Signal Generator and to help verify its functionality.

Connect the rear panel AC power to the AC mains (90 to 264 V_{AC}, 47 to 63 Hz). Then:

1. Push the power button "in" to turn on the unit.
   a. The model number will be briefly displayed
   b. Then the firmware version and unit serial number
   c. The unit will recall the its last operating state and begin operation

It is important to realize that the SG390 series signal generators resume operating with the same settings which were active when the unit was last turned off. There is a simple way to preset the instrument to a default state without changing any of the stored settings or the communications configuration: Notice that there is a "shifted function" above each key in the NUMERIC ENTRY portion of the key pad. To initialize the unit to its default settings, in the NUMERIC ENTRY section:

2. Press the [SHIFT] key
   a. The SHIFT LED will turn "on"
3. Press the number [0] (whose shifted function is "INIT")
   a. The display shows" Init. press enter"
4. Press the "ENTER" key (lowest, rightmost key [Hz % dBm])
   a. The instrument will be set to its default state

The default setting displays the frequency (10 MHz) and sets the AMPL of the BNC and Type N outputs to 0 dBm (1 mW into 50 Ω or 0.63 V_{PP}). Two green LEDs indicate that both the BNC and the Type N outputs are active, and another LED shows that the modulation is "OFF". The "LOCK" LED in the REF/SYNTH section should be "ON" (as should the "EXT" LED if the unit is connected to an external 10 MHz reference.)

Connect the front panel outputs to an oscilloscope. The oscilloscope timebase should be set for 50 ns/div and vertical sensitivity 200 mV/div with DC coupling and 50 Ω input impedance. The displayed cycle period should be 100 ns (2 divisions) and the displayed amplitude should be 630 mV_{PP}. (The displayed amplitude will be twice that if the oscilloscope input is not set for 50 Ω.)

Here are some things to try:

1. Change the frequency to 5 MHz by pressing [5] then [MHz V_{PP}]
2. Press the SELECT [◁] key six times to select the 1 MHz digit
3. Press the ADJUST [△] key to increase the frequency
4. Press the [AMPL] key to display the power at the Type N output
5. Press the ADJUST [△] key to increase the power by 1 dB
6. Press the [AMPL] key again to display the power at the BNC output
7. Press the [MHz V_{PP}] key to change the units from dBm to V_{PP}.
8. Press the ADJUST [△] key to increase amplitude by 0.100 V

The SG390 series generators also include a number of modulation presets which will automatically configure the generator to produce modulation waveforms for a number of different communications protocols, such as GSM, DECT, and TETRA. To access these presets, try the following:

1. Press [FREQ] [9] [3] [5] [.] [2] [MHz] to set the frequency to 935.2 MHz
2. Press [SHIFT] [FREQ] to access the modulation preset options.
3. Press the ADJUST [△] key successively until the display reads "GSM".
4. Press the ENTER key, [Hz], to configure the modulation.
5. Press [ON/OFF] to enable the modulation.

The SG390 will generate a GSM frame consisting of one TDMA slot of random data. Connect the rear panel, I/Q outputs, symbol clock, and event marker #1 to a scope. Trigger the scope on event marker #1 and set the time/div to 10 µs. The scope trace should look similar to that shown in Figure 27.

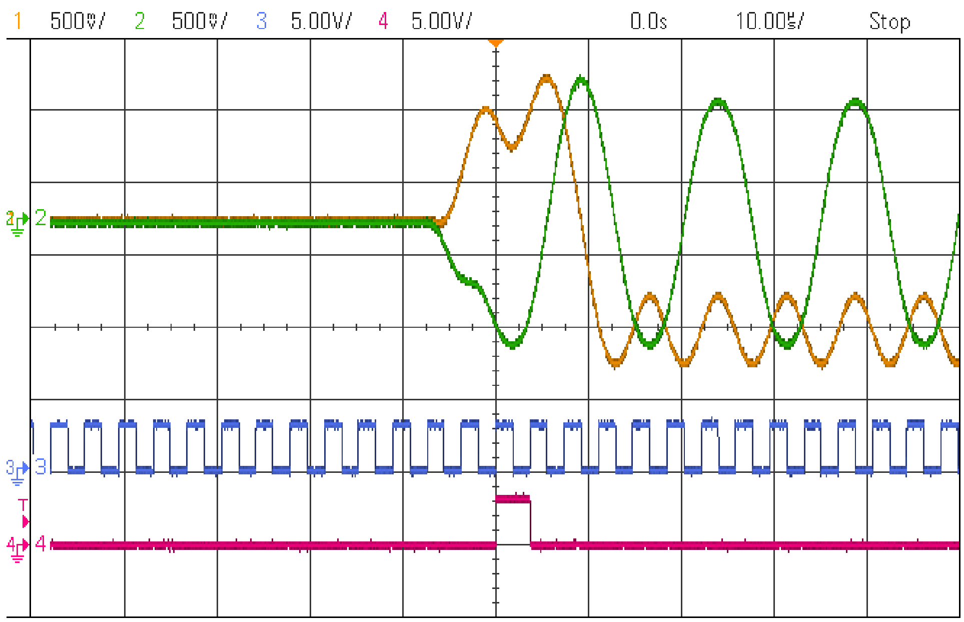


Figure 27: Example GSM scope trace

The scope traces show that before the TDMA slot begins the I and Q outputs are at ground, indicating that the RF power is off. Two symbols before the beginning of the time slot, the power is ramped up to full power. The beginning of data transmission for the time slot is indicated by event marker #1, which is trace 4 in the figure. The symbol clock shows the timing of symbol transmission relative to the I/Q outputs.

Introduction

Feature Overview

The SG392, SG394, and SG396 are a new series of RF vector signal generators that build upon the performance of the SG380 series of analog signal generators. Both series feature a new frequency synthesis technique that provides low phase noise, agile modulation, fast settling, and virtually infinite frequency resolution. The SG390 series augments this performance, however, with the inclusion of a dual baseband arbitrary waveform generator and built-in support for digital vector modulation.

Each of the generators has two front panel outputs with overlapping frequency ranges. The front panel BNC output provides sine wave signals from DC to 62.5 MHz with an adjustable DC offset, and amplitudes ranging from 1 mV_{RMS} to 1 V_{RMS}. The front panel Type N connector output provides AC coupled, sine wave signals from 950 kHz to 2.025 GHz (SG392), 4.050 GHZ (SG394), and 6.05 GHz (SG396) with power levels ranging from –110 dBm to +16.5 dBm.

Like the SG380 series the SG390 generators have extensive analog modulation capabilities available at all carrier frequencies. The front panel outputs can be amplitude, frequency, phase or pulse modulated by internally generated waveforms (sines, ramps, triangles, pulse and noise) or by external sources.

The SG390 series builds upon this performance by adding full support for vector signal modulation on RF carriers between 400 MHz and 6.075 GHz. It features a dual, arbitrary waveform generator operating at 125MHz for baseband signal generation. The generator has built-in support for the most common vector modulation schemes: ASK, QPSK, DQPSK, π/4 DQPSK, 8PSK, FSK, CPM. QAM (4 to 256), 8VSB, and 16VSB. It also includes built-in support for all the standard pulse shaping filters used in digital communications: raised cosine, root-raised cosine, Gaussian, rectangular, triangular, and more. Lastly, it provides direct support for the controlled injection of additive white Gaussian noise (AWGN) into the signal path.

The baseband generator supports the playback of pure digital data. It automatically maps digital symbols into a selected IQ constellation at symbol rates of up to 6 MHz and passes the result through the selected pulse shaping filter to generate a final waveform updated in real time at 125 MHz. This baseband signal then modulates the RF carrier using standard IQ modulation techniques.

This architecture leads to a greatly simplified and productive user experience. PRBS data and simple patterns can be played back directly from the front panel. Trade-offs in filter bandwidth versus power efficiency can be explored from the front panel in real time without the need to download complex new waveforms each time. Likewise, the degradation of a signal by AWGN can be easily manipulated from the front panel.

Although not directly configurable from the front panel, the SG390 series generators also support the generation of time domain, multiple access (TDMA) signals and event markers. Event markers enable the user to mark events during the playback of a waveform, such as the start of a frame, or a slot within a frame. Three rear-panel BNC outputs tied to these events may be programmed to pulse high or low for an arbitrary number of symbols in order to synchronize other instrumentation with the event. Any one of these event markers may be selected to control the RF power of the output, thereby creating an RF burst useful for implementing TDMA signals. The RF burst follows a raised cosine profile with a ramp rate that can be configured to be 1, 2, 4, or 8 symbols wide.

Naturally, the SG390 series instruments can be extended by the user if desired by downloading and storing up to ten custom constellations, filters, and waveforms each. Complex constellations involving rotating coordinate systems, or differential encoding are supported directly. Filters with up to 24 symbols of memory are supported. 2MB of flash is available for waveform storage and playback. Due to the fact that the SG390 performs the symbol mapping and pulse shaping in real time, this is enough space to store 2 MSym of QAM 256 data or 16 MSym of 1 bit FSK data. For a 3-bit GSM-EDGE waveform running at 270.833 kSym/s this is enough storage for over 20 seconds of playback data which is updated at 125 MHz. Playing back such a waveform using raw 16-bit values for I and Q at 125 MHz would require more than 9 GB of storage.

The SG390 series generators come with a number of modulation presets for demonstrating the various modulation capabilities of the instrument. Sample modulation waveforms and setups are included for communications standards such as NADC, PDC, DECT, APCO Project 25, TETRA, GSM, GSM-EDGE, W-CDMA and ATSC DTV.

The rear panel of the SG390 series instruments has two BNC outputs which provide a replica of the baseband signal being applied to the IQ modulator. Two more BNC inputs are available to the user for external IQ modulation support with over 200 MHz of RF modulation bandwidth.

The user interface provides single-key access to the most commonly adjusted synthesizer parameters (frequency, amplitude, phase, modulation rate, and modulation deviation.) In addition, there are three standard communication interfaces (GPIB, RS-232 and LAN) which allow for all instrument parameters to be remotely controlled.

The accuracy, stability, and low phase noise of the SG390 series is supported by two high quality timebases. The standard timebase uses a 3rd overtone, SC-cut ovenized 10 MHz resonator. In addition to its remarkable stability (<0.002 ppm 0° to 45°C), and low aging (<0.05 ppm/yr), this oscillator is responsible for the low phase noise close to carrier (–80 dBc/Hz at 10 Hz offset from a 1 GHz carrier) and its short term stability (1:10^{-11} 1s root Allan variance).

An optional rubidium timebase reduces the frequency aging to <0.001 ppm/yr. This timebase (an SRS PRS10 rubidium frequency standard) also improves the frequency stability to <0.0001 ppm over 0° to 45°C.

The 10 MHz output from the internal timebase is made available on a rear panel BNC connector. The user can also provide a 10 MHz timebase via a rear panel external timebase input.

Front-Panel Overview

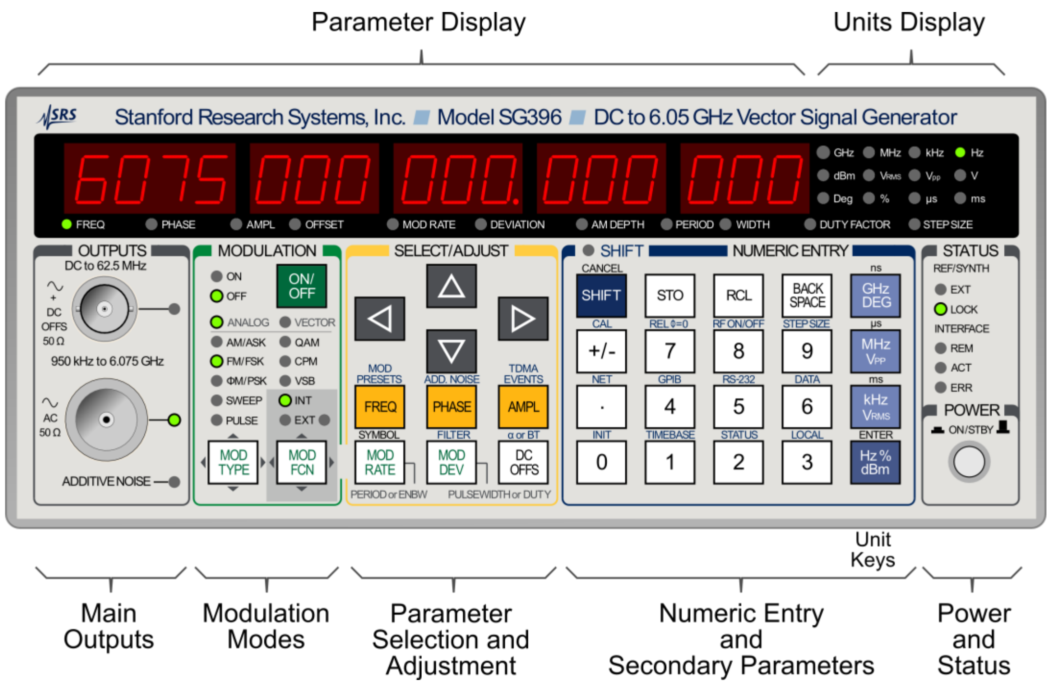


Figure 28: The SG396 front panel

The front panel operation of each SG390 series RF Signal Generator is virtually the same, with the only substantial difference being the model number and the maximum operating frequency.

The front panel is divided into seven sections: Parameter Display, Units Display, Outputs, Modulation, Select/Adjust, Numeric Entry, and Status as shown in Figure 28.

The power switch is located in the lower right corner of the front panel. Pushing the switch enables power to the instrument. Pushing the switch again places the instrument in stand-by mode, where power is enabled only to the internal timebase.

Parameter and Units Display

The front panel has a sixteen digit display showing the value of the currently displayed parameter. The LEDs below the display indicate which parameter is being viewed. The units associated with a parameter are highlighted at the right. Some parameters may have multiple views. The RF output amplitude, for example, may be viewed in units of dBm, V_{RMS}, or V_{PP}.

Main Outputs

These are the synthesizer's main signal outputs. Two types of connectors are provided due to the bandwidths covered by the instrument.

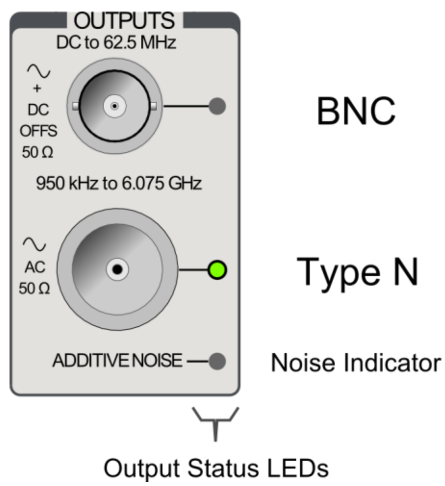


Figure 29: The SG396 front panel outputs.

BNC Output

Signals on this connector are active for frequency settings between DC and 62.5 MHz. The amplitude may be set independently for levels from 1 mV_{RMS} to 1 V_{RMS} (–47 dBm to 13 dBm). Increased amplitude settings of 1.25 V_{RMS} (14.96 dBm) are allowed with relaxed signal specifications. Additionally, the BNC output may be offset by ±1.5 V_{DC}, however non-zero offsets will reduce the maximum amplitude setting. The BNC output is protected against externally applied voltages of up to ±5 V.

Type N Output

Signals on this connector are active for frequency settings between 950 kHz and 2.025 GHz, 4.050 GHz, or 6.075 GHz (for the SG392, SG394 and SG396 respectively). The output power may be set from −110 dBm to 16.5 dBm (0.7 μV_{RMS} to 1.5 V_{RMS}). The maximum output power is reduced by 3.50 dB/GHz above 3 GHz for the SG394, or by 3.25 dB/GHz above 4 GHz for the SG396. The Type N output is protected against externally applied voltages of up to 30 V_{DC} and RF powers up to +25 dBm.

Indicators

Two LEDs are used to indicate which of the outputs are active: BNC and/or Type N. A third LED indicates if a modulated waveform has been degraded by additive white Gaussian noise (AWGN).

Modulation Modes

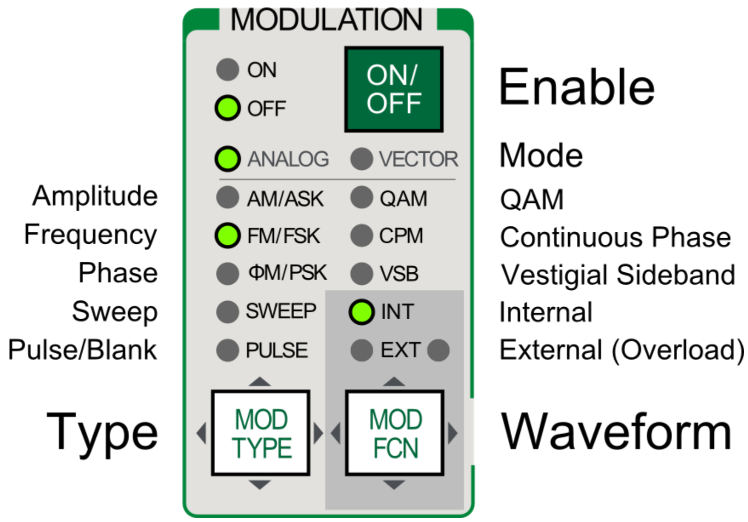


Figure 30: The SG396 front panel modulation section.

The Modulation section displays the present modulation state and enables the user to control both the type and function of the modulation.

The [ON/OFF] key enables modulation.

The [MOD TYPE] key allows selection of the type of modulation. Use the ADJUST [△] and [▽] keys to select the preferred type of modulation: AM, FM, ΦM, etc. Use the SELECT [◁] and [▷] keys to select the subtype of modulation: analog, vector, and constellation (bits/Symbol).

The [MOD FCN] key allows the selection of the modulation waveform. Use the ADJUST [△] and [▽] keys to select the desired waveform: sine, ramp, triangle, user, etc. Use the SELECT [◁] and [▷] keys to modify the selected waveform if appropriate. The PRBS length and symbol pattern are modified this way.

The SG390 series generators support two different modes of modulation: analog and vector. The front panel LEDs for ANALOG and VECTOR highlight which type of modulation is active. When analog modulation is selected, modulation waveforms are replicated on the rear panel ANALOG MOD output. Similarly, when vector modulation is selected, modulation waveforms are replicated on the VECTOR MOD I and Q outputs.

Modulation waveforms may be internally or externally generated. The INT and EXT LEDs indicate which source is active. Internally generated waveforms include sine, ramp, triangle, square, noise, and user arbs. The rear panel external modulation input can also be used in AM, FM, ΦM or Pulse modulations. When external modulation is selected, apply an external signal source to the rear panel ANALOG MOD input for analog modulation. Apply it to the rear panel VECTOR MOD I and Q inputs for vector modulation.

For all types of modulation, the instrument will monitor the input for overloads. If the source exceeds operational limits or was digitally clipped, the red overload LED on the right side of the EXT label will flash.

Parameter Selection and Adjustment

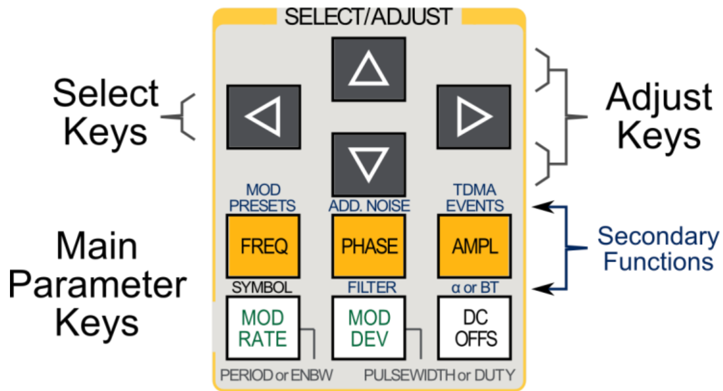


Figure 31: The SG396 front panel parameter selection and adjustment section.

Display Navigation

The SELECT/ADJUST section determines which main parameter is shown on the front panel display. The six basic displays for viewing and modifying instrument settings are shown in Table 1. Each display is activated by pressing the correspondingly labeled key.

Table 1: Main Parameter Keys

Label	Value Shown in Main Display When Pressed
FREQ	Carrier frequency (f_c)
PHASE	Phase
AMPL	Amplitude or power— Type N or BNC output
DC OFFS	DC offset — BNC output
MOD RATE	Modulation or symbol rate, pulse period, or noise bandwidth
MOD DEV	Modulation deviation, pulse width or duty cycle)

For parameter menus with multiple items, repeated presses of a key will cycle through all available items. For example, in the default configuration multiple key presses of the [AMPL] key will cycle through the various available outputs BNC, and Type N.

Some of the parameters will have a blinking digit (the cursor). The cursor indicates which digit will be modified when the ADJUST [△] and [▽] keys are pressed. The SELECT [◁] and [▷] keys allow adjusting the cursor for the desired resolution. The step size may also set via the STEP SIZE secondary function and a numeric entry (to set channel spacing, for example.)

Numeric Entry and Secondary Parameters

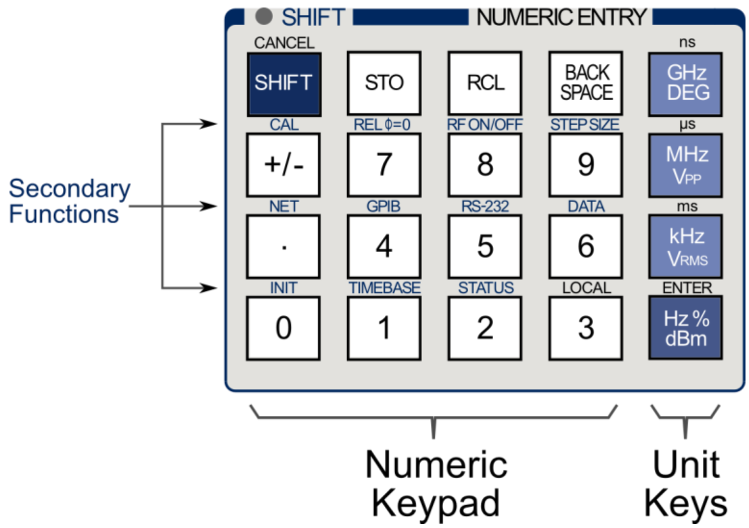


Figure 32: The SG396 front panel numeric entry section.

This section is used for changing the currently displayed numeric parameter directly. A parameter is entered numerically and completed by pressing any of the unit keys. Corrections can be made using the [BACK SPACE] key, or the entire entry may be aborted by pressing [SHIFT (CANCEL)].

For example, to set the frequency to 1.0001 GHz, press the [FREQ] key followed by the key sequence of [1] [•] [0] [0] [0] [1] [GHz].

This section also allows access to secondary or shifted functions. The secondary functions are listed above the key in light blue text. A secondary function is accessed by first pressing the [SHIFT] key (indicated by the SHIFT LED being on) followed by pressing the desired secondary function key.

For example, to force the instrument to default settings, sequentially press the keys [SHIFT] [0 (INIT)] [ENTER].

Stepping Up and Down

Most instrument settings can be stepped up or down by a programmed amount. The blinking digit identifies the current cursor position and step size. The cursor shows the digit that will change if the parameter is incremented or decremented via the ADJUST keys. Pressing the ADJUST [△] or [▽] keys cause the displayed parameter to increment or decrement, respectively, by the current step size.

Step Size

Pressing the ADJUST [△] and [▽] keys increments or decrements the value of the selected digit on the numeric display. Use the SELECT [◁] and [▷] keys to move the cursor to the desired digit.

The step size can be changed to an arbitrary value via the secondary function STEP SIZE and the numeric keypad. Press [SHIFT] [9 (STEP SIZE)] and enter the desired step size followed by the appropriate unit type. For example, to change the frequency's step size to 1.25 MHz, first press [SHIFT] [9] followed by [1] [•] [2] [5] [MHz].

Subsequent use of the SELECT [◁] or [▷] keys will return the step size to the nearest factor of ten.

Store and Recall Settings

The [STO] and [RCL] keys are for storing and recalling instrument settings, respectively. Instrument settings include modulation configuration and all associated step sizes. Up to nine different instrument settings may be stored in the locations 1 to 9. To save the current settings to location 5, the user should sequentially press the keys [STO] [5] [ENTER]. To later recall instrument settings from location 5, the user should sequentially press the keys [RCL] [5] [ENTER]. Note that location 0 is reserved for recalling default instrument settings. Default instrument settings can also be recalled via the INIT secondary function. For additional details, see Factory Default Settings in the Basic Operation chapter starting on page 25.

Secondary Functions

Many of the keys in the NUMERIC ENTRY and SELECT/ADJUST sections have secondary (or SHIFT) functions associated with them. The secondary functions are listed above the keys. The [5] key, for example, has RS-232 above it.

The secondary functions can only be accessed when SHIFT mode is active, which is indicated by SHIFT LED in the main display. The SHIFT mode can be toggled on and off by pressing the [SHIFT] key. For example, to access the RS-232 communications configuration menu, press [SHIFT] [5].

For menu items with multi-parameter settings, the SELECT [◁] and [▷] keys allow selection of the various menu items. The ADJUST [△] and [▽] keys may be used to modify a parameter. For example, the first option in the RS-232 menu is RS232 Enable/Disable. Use the ADJUST [△] and [▽] keys to change the setting as desired. Then press SELECT [▷] to move to the next option which is baud rate. Continue pressing the SELECT [▷] until all settings have been configured as desired.

A detailed description of all the secondary functions can be found in the Secondary Functions section of the Basic Operation chapter starting on page 19.

Cancel

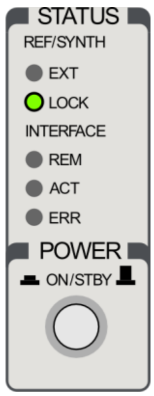
The [SHIFT] key also functions as a general purpose CANCEL key. Any numeric entry, which has not been completed, can be canceled by pressing the [SHIFT] key. Because of the dual role played by the SHIFT key, the user may have to press [SHIFT] twice to reactivate SHIFT mode. The first key press cancels the current action, and the second key press re-activates SHIFT mode.

Power and Status

The Power and Status section encompass the power switch and displays the status of the timebase and remote interface(s):

Status Indicators

REF / SYNTH



On the far right portion of the front panel are two groups of LED indicators. The upper group is labeled REF / SYNTH and indicates the status of the internal timebase. The EXT LED indicates that the instrument has detected an external 10 MHz reference at the timebase input BNC on the rear panel. If detected, the instrument will attempt to lock its internal clock to the external reference.

The LOCK LED indicates that unit has locked its internal frequency synthesizer at the requested frequency. Normally this LED will only extinguish momentarily when the frequency changes or an external timebase is first applied to the rear input. If the LED stays off, it indicates that the signal generator may be unable to lock to the external timebase. This is most commonly caused by the external frequency being offset by more than 2 ppm from 10 MHz.

INTERFACE

The lower group of LED indicators is labeled INTERFACE. These LEDs indicate the current status of any active remote programming interface (Ethernet, RS-232, or GPIB).

The REM (remote) LED turns on when the unit is placed in remote mode by one of the remote interfaces. In this mode, all the front panel keys are disabled and the instrument can only be controlled via the remote interface. The user can return to normal, local mode by pressing the [3] key (also labeled [LOCAL]). The ACT (activity) LED flashes when a character is received or sent over one of the interfaces. This is helpful when troubleshooting communication problems. If a command received over the remote interface fails to execute due to either a parsing error or an execution error, the ERR (error) LED will turn on. Information about the error is available in the STATUS secondary display. See page 24 for more detailed information on how to access this display.

POWER

The power switch has two positions: STANDBY (button out) and ON (button in).

In STANDBY mode, power is only supplied to the internal timebase and the power consumption will not exceed 25 watts. In ON mode, power is supplied to all circuitry and the instrument is on.

Rear-Panel Overview

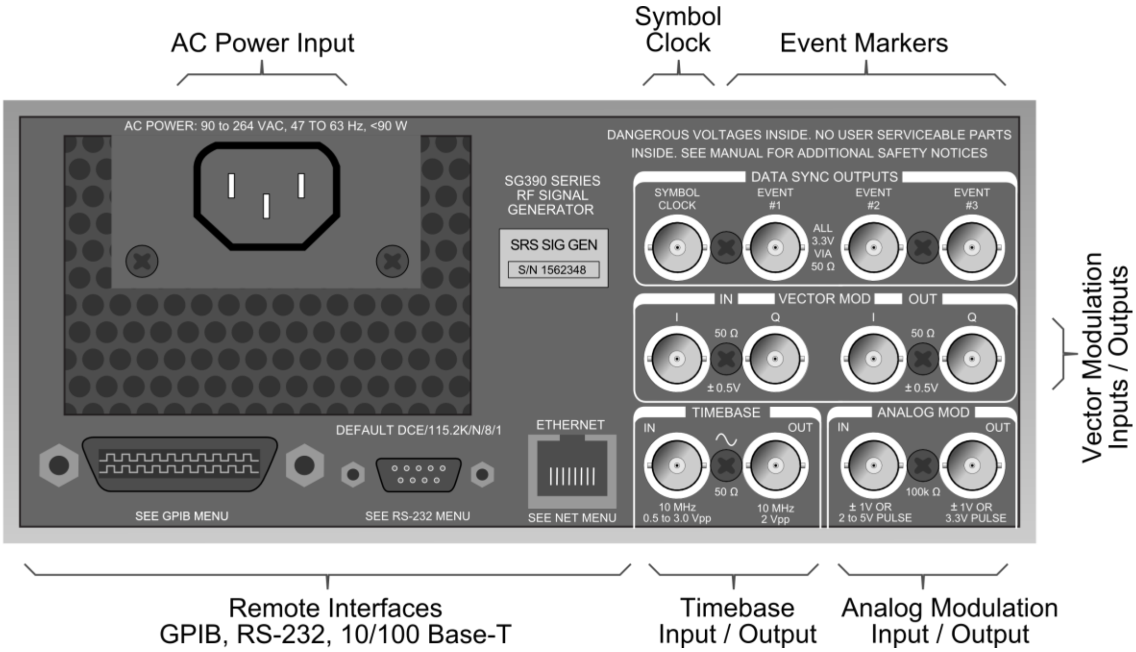


Figure 33: The SG396 Rear Panel

The rear panel provides connectors for AC power, remote computer interfaces, external frequency references, modulation, and data synchronization.

AC Power

Connect the unit to a power source through the power cord provided with the instrument. The center pin is connected to the chassis so that the entire box is earth grounded. The unit will operate with an AC input from 90 to 264 V, and with a frequency of 47 to 63 Hz. The instrument requires 90W and implements power factor correction. Connect only to a properly grounded outlet. Consult an electrician if necessary.

Remote Interfaces

The instruments support remote control via GPIB, RS-232, or Ethernet. A computer can perform any operation that is accessible from the front panel. Programming the instrument is discussed in the Remote Programming chapter. Please refer to the Interface Configuration section starting on page 87, before attempting to communicate with the signal generators via any computer interface.

GPIB

The signal generators have a GPIB (IEEE-488) communications port for communications over a GPIB bus. The instruments support the IEEE-488.1 (1978) interface standard. It also supports the required common commands of the IEEE-488.2 (1987) standard.

RS-232

The RS-232 port uses a standard 9 pin, female, subminiature-D connector. It is configured as a DCE and supports baud rates from 4.8 kb/s to 115 kb/s. The remaining communication parameters are fixed at 8 Data bits, 1 Stop bit, No Parity, with RTS/CTS configured to support Hardware Flow Control.

Ethernet

The Ethernet uses a standard RJ-45 connector to connect to a local area network (LAN) using standard Category-5 or Category-6 cable. It supports both 10 and 100 Base-T Ethernet connection and a variety of TCP/IP configuration methods.

Timebase

10 MHz IN

This input accepts an external 10 MHz reference. The external reference should be accurate to at least 2 ppm, and provide a signal of no less than 0.5 V_{PP} while driving a 50 Ω impedance. The instrument automatically detects the presence of an external reference, asserting the front panel EXT LED, and locking to it if possible. If the unit is unable to lock to the reference, the LOCK LED is turned off.

10 MHz OUT

The instrument also provides a 10 MHz output for referencing other instrumentation to the internal high stability OCXO or optional rubidium timebase.

Analog Modulation

IN

External analog modulation is applied to this input. The input impedance is 100 kΩ with a selectable input coupling of either DC or AC (4 Hz roll off).

For analog modulations (AM, FM, ΦM), a signal of ±1 V will produce a full scale modulation of the output (depth for AM or deviation for FM and ΦM). It supports bandwidths of 100 kHz and introduces distortions of less than –50 dB.

For Pulse/Blank modulation types, this input is used as a discriminator that has a fixed threshold of +1 V.

OUT

This output replicates the analog modulation waveform and has a 50 Ω reverse termination. When using the internal source for AM, FM, and ΦM, it provides a waveform determined by the function and rate settings with an amplitude of ±1 V_{PP} into a high impedance. During external analog modulation, this output mirrors the modulation input.

For Pulse modulation, the output is a 3.3V logic waveform that coincides with the gate signal.

Vector Modulation

Vector modulation on the front panel, Type N RF output is supported for carrier frequencies above 400 MHz. The modulation source may be an external signal or the internal baseband generator. The desired source may be selected via the [MOD FCN] key and the ADJUST [△] and [▽] keys on the front panel.

IN

These BNC inputs enable external I/Q modulation. They accept signals of ±0.5 V, corresponding to full scale modulation, and have 50 Ω input impedances. Both inputs support signal bandwidths from DC to 100 MHz providing an RF modulation bandwidth of up to 200 MHz

OUT

These BNC outputs replicate the baseband I/Q modulation waveforms currently being used to modulate the RF. Both outputs have a source impedance of 50 Ω and when terminated into 50 Ω, will generate a full scale output of ±0.5 V.

Data Sync Outputs

The SG390 series generators include a built-in baseband generator which can play back pure digital data at symbol rates of up to 6 MHz and pass the result through a pulse shaping filter which is updated at 125 MHz. To enable synchronization of external instrumentation with the modulation, the symbol clock and three event markers are available on the rear panel.

Symbol Clock

This BNC output provides a square wave synchronized to the symbol clock used in the modulation. The rising edge of this clock triggers the programmed event markers associated with the arbitrary waveform.

Events

Three BNC outputs labeled #1, #2, and #3 are available for synchronizing external instrumentation to programmable events within a generated arbitrary waveform. These may be programmed, for instance, to mark the start of a frame, or a slot within a frame, or the start of a synchronizing pattern in the waveform. One of the event markers may be further programmed to control the RF power of the front panel output for the generation TDMA signals. Events are triggered on the rising edge of the symbol clock.

Basic Operation

Introduction

The previous chapter provided an overview of the instrument's features. This chapter describes the setting of the frequency, phase, and amplitude as well as the details of storing and recalling setups, and executing secondary functions.

Power-On

At power on, the unit will briefly display the model number followed by the firmware version and the unit serial number. When power on initialization has completed, the instrument will recall the last operational settings from nonvolatile memory.

The instrument continuously monitors front panel key presses and will save the current instrument settings to nonvolatile memory after approximately two seconds of inactivity. To prevent the nonvolatile memory from wearing out, the unit will not automatically save instrument settings that change due to commands executed over the remote interface. The remote commands *SAV (*RCL) may be used to explicitly save (recall) instrument settings over the remote interface, if desired. (See the Remote Programming section for more information about these commands.)

The signal generator can be forced to revert to factory default settings. This is accomplished by power cycling the unit with the [BACK SPACE] depressed. All instrument settings, except for the remote interface configurations, will be set back to their default values. Warning: this will also delete all downloaded user waveforms, constellations, and filters. See Factory Default Settings starting on page 25 for a list of default settings.

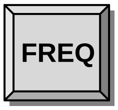
Setting Parameters

The SELECT/ADJUST section determines which parameter is shown in the main front panel display. The six keys for selecting the display of the main instrument settings are shown in Table 2. Each display is activated by pressing the corresponding labeled key. Use the SELECT [◁] and [▷], and ADJUST [△] and [▽] keys to modify a displayed parameter.

Table 2: Main Display Parameters

SELECT Key	Displayed Value
FREQ	Carrier frequency (f_c)
PHASE	Phase
AMPL	Amplitude or power — Type N or BNC output
DC OFFS	Offset — BNC output, or internal I/Q offset
MOD RATE	Modulation or symbol rate, pulse period, or noise bandwidth
MOD DEV	Modulation deviation, pulse width, or duty factor

Frequency



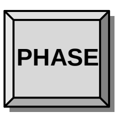
Pressing [FREQ] displays the carrier frequency of the front panel outputs. A frequency may be entered in any of the following units: GHz, MHz, kHz, or Hz. For example, to set the frequency to 5 MHz, press the keys [FREQ] [5] [MHz]. The frequency resolution is 1 µHz at all frequencies. The units for the displayed frequency may be changed by pressing the desired unit key. For example, to change the display from units of MHz to Hz simply press the [Hz] key.

The frequency setting determines which outputs may be active at any given time. The green LED next to the front panel outputs indicate which outputs are enabled. None of the outputs operate across the entire frequency range. Table 3 shows the frequency ranges over which each front panel output is active for each model in the series.

Table 3: Frequencies of Operation

Model	**SG392**	**SG394**	**SG396**
Front BNC	DC-62.5 MHz	DC-62.5 MHz	DC-62.5 MHz
Type N	950 kHz to 2.025 GHz	950 kHz to 4.050 GHz	950 kHz to 6.075 GHz

Phase



Pressing [PHASE] displays the output's relative phase. The phase is displayed in degrees and is adjustable over ±360º. If the phase adjustment exceeds 360º, the phase is displayed modulo 360º. The displayed phase is reset to 0° whenever the carrier frequency is changed.

The phase resolution depends upon the current setting of the frequency. For frequencies up to 100 MHz the phase resolution is 0.01°, with reduced resolution for higher frequencies. Table 4 shows the phase resolution verses frequency:

Table 4: Phase Resolution

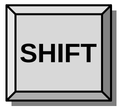
Frequency Range	**Phase Resolution**
DC to 100 MHz	0.01°
100 MHz to 1 GHz	0.1°
1 GHz to 6.075 GHz	1.0°

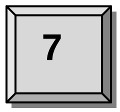
Changing the phase changes the phase of all outputs from the synthesizer. This sometimes makes it difficult to see that you have done anything at all. Phase adjustments are usually only made when there are more than one signal source in a measurement situation. For example, if you have two RF synthesizers, each connected to the same external 10 MHz timebase and set to the same frequency, you will be able to see their relative phase by viewing them simultaneously on an oscilloscope or by applying them both to a mixer and measuring the mixer's IF output.

You can also see phase changes (for frequencies which are a multiple of 10 MHz) by viewing the signal on an oscilloscope while triggering the oscilloscope from the rear panel 10 MHz timebase output.

Finally, you can see the phase adjustment by viewing the RF signal in a polar display of a vector signal analyzer. It is important to ensure that the vector signal analyzer and the RF synthesizer share the same timebase in this setup.

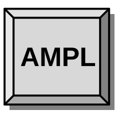
Rel Phase





In many situations it is useful to be able to define the present phase setting as 0°. The REL Φ=0 secondary function enables this feature. Pressing the keys [SHIFT] [7] will REL the phase display to zero without modifying current phase of the either front panel RF output.

Amplitude and Power



Pressing [AMPL] displays the output amplitude or power of the displayed output. Repeated presses of [AMPL] sequences through the available RF outputs: Type N and BNC. Note, however, that only outputs that are active for the current frequency setting will be accessible. If an output is set below its minimum value it will be disabled. This is indicated on the display as "off" and by extinguishing the LED which is next to the output.

All amplitudes may be displayed in units of dBm, V_{RMS}, or V_{PP}. All stated values assume a load termination of 50 Ω. Output amplitudes will (approximately) double if not terminated.

The units used for the displayed power or amplitude may be changed with a single key press. For example, if the Type N output power is displayed as 0.00 dBm, pressing the [V_{RMS}] key will display 0.224 V_{RMS} and pressing the [V_{PP}] key will display 0.632 V_{PP}.

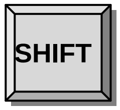
Table 5 lists the range for the various units of the outputs:

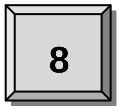
Table 5: Output Power Ranges

Output	Power	Amplitude (V_{RMS})	Amplitude (V_{PP})
Front Type N (1) (2)	–110 dBm → +16.5 dBm	0.707 µ → 1.50 V_{RMS}	2 µ → 4.24 V_{PP}
Front BNC (3)	–47 dBm → +13 dBm	0.001 → 1.000 V_{RMS}	.0028 → 2.82 V_{PP}

(1) For the SG394 the maximum power is reduced by 3.50 dB/GHz above 3 GHz. (The maximum power available at 4 GHz is 13 dBm.)
(2) For the SG396 the maximum power is reduced by 3.25 dB/GHz above 4 GHz. (The maximum power available at 6 GHz is 10 dBm.)
(3) The amplitude of the BNC may be set as high as 1.25 V_{RMS} (+14.96 dBm), with reduced distortion specifications, provided that the BNC DC offset is set to 0 V.

RF ON/OFF





The front panel outputs may be turned on and off via the secondary function RF ON/OFF. Press the keys [SHIFT] [8] and then use the ADJUST [△] and [▽] keys to toggle the power on and off. When the RF is off, the LEDs associated with each output will be off. See Figure 29 on page 6. The amplitude display for each output will also indicate that is off.

DC Offset

Pressing [DC OFFS] displays output offset voltages. On the front panel, only the BNC output has a settable DC offset. The Type N RF output is AC coupled and so has no DC offset setting. The DC offset for the front panel BNC is always accessible and active (independent of the frequency setting). Table 6 gives the DC offset range for the front panel outputs:

Table 6: Offset Range

Output	DC Offset Range
Type N	N/A
BNC	±1.5V

The BNC output will support offsets up to 1.5V. The output is very linear over ±1.9V while driving a 50 Ω load. To maintain low distortion of AC signals in the presence of a DC offset it is necessary to reduce the amplitude of the AC signal. The output provides 13 dBm (2.828 V_{PP}) at no offset, and is reduced linearly to 0 dBm (0.632 V_{PP}) for offsets of ±1.5 V. Table 7 shows the allowed amplitude (or power settings) for the BNC output for various DC offsets:

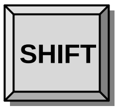
Table 7: BNC Output vs. DC Offset

BNC DC Offset	Max Output (V_{PP})	Max Output (V_{RMS})	Max Output (dBm)
0.00 V	2.83 V_{PP}	1.00 V_{RMS}	13.01 dBm
±0.25 V	2.46 V_{PP}	0.871 V_{RMS}	11.81 dBm
±0.50 V	2.10 V_{PP}	0.741 V_{RMS}	10.41 dBm
±0.75 V	1.73 V_{PP}	0.612 V_{RMS}	8.75 dBm
±1.00 V	1.37 V_{PP}	0.483 V_{RMS}	6.69 dBm
±1.25 V	0.998 V_{PP}	0.353 V_{RMS}	3.97 dBm
±1.50 V	0.634 V_{PP}	0.224 V_{RMS}	0.02 dBm

IQ Modulation Offsets

The [DC OFFS] button also allows one to adjust the IQ offset for internally generated vector modulations. Each channel, I and Q, may be offset by up to 5% of the carrier amplitude. For example, to set the I channel offset to 1.5%, press [DC OFFS] successively until the display reads “I offset.” Then press the keys [1] [.] [5] [%] to set the offset.

Secondary Functions



Many of the keys in the SELECT/ADJUST and NUMERIC ENTRY sections of the front panel have secondary functions associated with them. The text above the key identifies the secondary function associated with it. For example, the [4] key has the label RS-232 in blue text above it. Table 8 summarizes the keys and their secondary functions.

Table 8: Shifted Key Functions

Label	Primary Key	Function Description
MOD PRESETS	FREQ	Configure the instrument to perform one of a number of preset modulation waveforms.
ADD. NOISE	PHASE	Add noise to a modulation waveform
TDMA EVENTS	AMPL	View the TDMA configuration for the current modulation waveform
FILTER	MOD DEV	Select the pulse shaping filter for the current modulation waveform.
α or BT	DC OFFS	Adjust the bandwidth of nyquist, root nyquist and Gaussian filters.
CAL	+/-	Selects the PLL filter mode and adjust timebase calibration
REL Φ =0	7	Defines the current phase to be 0 degrees and displays phase parameter (of 0)
RF ON/OFF	8	Turn RF power to the front panel outputs on or off.
STEP SIZE	9	Set the incremental value used by the ADJUST keys
NET	•	Configure ethernet interface
GPIB	4	Configure GPIB interface
RS-232	5	Configure RS-232 interface
DATA	6	Display the most recent data received over any remote interface
INIT	0	Load default instrument settings
TIMEBASE	1	Displays the timebase configuration
STATUS	2	View TCP/IP (Ethernet), error, or instrument status, as well as running Self-Test
LOCAL	3	Go to local. Enables front panel keys if the unit is in remote mode.

MOD PRESETS

The modulation preset menu, [SHIFT] [FREQ], enables one to configure the instrument to perform one of a number of preset modulation waveforms as summarized in Table 9. Use the ADJUST [△] and [▽] keys to select the desired modulation waveform and press [ENTER] to update instrument settings.

Table 9: Modulation presets

Label	Modulation Description
AM Audio	Analog AM modulation of an audio clip.
FM Audio	Analog FM modulation of an audio clip.
NADC	Vector modulation parameters used in North American Digital Cellular (NADC) communications.
PDC	Vector modulation parameters used in Personal Digital Cellular (PDC) communications.
DECT	One TDMA slot within one frame of random data using the vector modulation parameters of Digital Enhanced Cordless Telecommunications (DECT). The waveform transmits a P32 packet which includes the Z field and is 424 symbols long.
APCO 25	Vector modulation parameters used in the APCO Project 25 communications system.
TETRA	One TDMA slot within one frame of random data using the vector modulation parameters used in Terrestrial Trunked Radio (TETRA) communications. The waveform transmits a normal up-link burst, 231 symbols long, using normal training sequence 1.
GSM	One TDMA slot within one frame of random data using the vector modulation parameters of the Global System for Mobile communications (GSM). The packet is 148 symbols long and the midamble is filled with training sequence 0.
GSM EDGE	One TDMA slot within one frame of random data using the vector modulation parameters of the GSM with Enhanced Data rate for GSM Evolution (GSM-EDGE) communications. The packet is 148 symbols long and the midamble is filled with training sequence 0.
Wide-CDMA	One frame with one control channel and six data channels of random data using the vector modulation parameters of Wideband Code Division Multiple Access (W-CDMA) communications for an uplink channel in a frequency division duplex (FDD) installation. The control channel uses a spreading factor of 256 while the data channels use a spreading factor of 4. The control and data channels are scrambled with long scrambling code 0.
ATSC DTV	Vector modulation parameters used in the Advanced Television Systems Committee, Inc (ATSC) Digital Television Standard for over-the-air broadcast of digital television.

The presets configure the instrument to perform the selected modulation, but the modulation is turned off. The user will need to enable the modulation by pressing the front panel [ON/OFF] key in the MODULATION section of front panel. Non-modulation parameters, such as frequency and amplitude, are not modified by the presets. The one exception is that the frequency will be set to 1 GHz if the current frequency is below 400 MHz and the selection is a vector modulation format, which requires the frequency to be above 400 MHz.

ADD. NOISE

The additive noise menu, [SHIFT] [PHASE], enables one to degrade a vector modulation waveform with additive white Gaussian noise (AWGN). The noise menu options are summarize in Table 10.

Table 10: Additive Noise Menu

Parameter	Description
Added Noise	Configure added noise off, on, or only.
Noise Power	Noise power relative to full scale carrier power.

Noise may be added to vector modulation waveforms and to arbitrary user waveforms for analog modulation. Use the ADJUST [△] and [▽] keys to select between noise options: off, on, and only. The "noise only" option enables one to turn off the signal and pass only the added noise. If desired. Use the SELECT [▷] to view and adjust the noise power. Enter the desired noise power via the numeric key pad. Noise powers from -10 dB to -70 dB relative to full scale carrier power may be entered. This gives one the ability to create typical error vector magnitudes (EVM) ranging from 32 % to 0.32 %, respectively.

TDMA EVENTS

The TDMA events menu, [SHIFT] [AMPL], allows one to view the current TDMA configuration. TDMA events may only be programmed via the remote interface. However, this menu enables one to view the current TDMA configuration which is summarized in Table 11. Use the SELECT [◁] and [▷] keys to switch between parameters. TDMA events may only be programmed for vector modulated waveforms.

Table 11: TDMA configuration parameters

Parameter	Description
TDMA on/off	Indicates if TDMA is on or off.
TDMA ramp	Indicates the number of symbols over which the RF power ramps from minimum to maximum power.
TDMA event	Indicates which rear panel event marker output (1, 2 or 3) is tied to the RF power to implement the TDMA power burst.

FILTER

The filter menu, [SHIFT] [MOD DEV], allows one to select the pulse shaping filter to use for waveform playback. The available options are summarize in Table 12. Use the ADJUST [△] and [▽] keys to select the desired filter. The first three filters listed actually represent three families of filters for which the bandwidth of the filter may be adjusted. See the secondary function "α or BT" described below to adjust the bandwidth of the selected filter.

Table 12: Pulse shaping filters

Filter	Description
Nyquist	Raised cosine filter. Use the “α or BT” secondary function to set the bandwidth of the filter.
Root Nyquist	Root-raised cosine filter. Use the “α or BT” secondary function to set the bandwidth of the filter.
Gaussian	Gaussian filter. Use the “α or BT” secondary function to set the bandwidth of the filter.
Rect	Rectangular filter.
Triangle	Triangular filter. This is equivalent to linear interpolation between data points.
Win. Sinc	Sinc(x) filter windowed by a Kaiser function with β=7.85.
Lin Gauss	Linearized Gaussian filter described in the modulation specification for GSM-EDGE.
C4FM	Raised cosine filter with $\alpha = 0.2$ cascaded with an inverse Sinc(x) filter. This filter is described in the APCO Project 25 specification.
User RAM	Custom user filter stored in SRAM
User 1 to 9	Up to 9 custom user filters stored in nonvolatile memory.

α or BT

This menu, [SHIFT] [DC OFFS], enables one to control the bandwidth of the raised cosine, root-raised cosine, and Gaussian filters. The parameters are summarized in Table 13. Use the numeric keypad to enter the desired filter factor.

Table 13: Filter bandwidth control parameters.

Filter	Parameter	Description
Nyquist	α	Excess bandwidth factor for the filter. May range from 0.1 to 1.0.
Root-nyquist	α	Excess bandwidth factor for the filter. May range from 0.1 to 1.0.
Gaussian	BT	Bandwidth symbol time product. May range from 0.1 to 1.0.

CAL

The cal menu, [SHIFT] [+/–], allows access to the RF PLL Noise Mode setting and the internal timebase calibration. The RF PLL Mode has two settings RF PLL 1 and 2. RF PLL 1 optimizes the noise floor of the output within 100 kHz of the carrier. This is the default setting. RF PLL 2 optimizes the noise floor of the output for offsets greater than 100 kHz from carrier. See Single Sideband Phase Noise vs RF PLL Mode on page xx of the Specifications for spectra showing the different characteristics of the two PLL modes.

The timebase calibration parameter allows adjustment of the timebase over a range of ±2 ppm (10 MHz ± 20 Hz). See the section Timebase Calibration on page 143 for details on how to calibrate the internal timebase.

REL Φ=0

[SHIFT] [7] sets the phase display to 0°. The phase of the output is not changed.

RF ON/OFF

[SHIFT] [8] enables the user to toggle the RF power of the front panel outputs on and off using the ADJUST [△] and [▽] keys. When the RF is off, the LEDs associated with each output will be off (see Figure 29 on page 6). The amplitude display for each output will also indicate that is off.

STEP SIZE

The step size menu, [SHIFT] [9], allows one to set an arbitrary step size for the ADJUST [△] and [▽] keys of a displayed parameter, such as frequency, phase, amplitude, etc. The default step size is ±1 at the blinking digit. Use the numeric keypad followed by a units key to enter a specific step size. For example, to set the frequency step size to 25 kHz, press [FREQ] [SHIFT] [9] followed by [2] [5] [kHz].

NET

The NET menu, [SHIFT] [•], enables the user to configure the TCP/IP based remote interfaces (the IP address, subnet mask, and default router). To see the current TCP/IP parameters use the STATUS menu. Before connecting the instrument to your LAN, check with your network administrator for the proper configuration of devices on your network.

This menu is discussed in detail in the Interface Configuration section of the Remote Programming chapter starting on page 87.

GPIB

The GPIB menu, [SHIFT] [4], enables the user to configure the GPIB remote interface. This menu is discussed in detail in the Interface Configuration section of the Remote Programming chapter starting on page 87.

RS-232

The RS-232 menu, [SHIFT] [5], enables the user to configure the RS-232 remote interface. This menu is discussed in detail in the Interface Configuration section of the Remote Programming chapter starting on page 87.

DATA

The DATA function, [SHIFT] [6], enables the user to see the hexadecimal ASCII characters received by the instrument from the most recently used remote interface. This functionality is useful when trying to debug communication problems. Use the ADJUST [△] and [▽] keys to scroll through the data. The decimal point indicates the last character received.

INIT

Executing the INIT function, [SHIFT] [0] [ENTER], forces the instrument to default settings. This is equivalent to a Recall 0 or executing the *RST remote command. See Factory Default Settings on page 25 for a list of the unit's default settings.

TIMEBASE

The timebase menu, [SHIFT] [1] shows the installed timebase. This can be the standard ovenized crystal oscillator (OCXO) or an optional rubidium oscillator. These parameters are summarized in Table 14

Table 14: Timebase Status Menu

Parameter	Example Display	Description
Oscillator	'Osc. ovenized'	Indicates which type of timebase is installed.
Rb lock	'Rb stable'	If a rubidium timebase is installed, this item indicates if the rubidium has stabilized.

STATUS

The status menu, [SHIFT] [2], enables the user to view status information. The instrument has four status menus: TCP/IP status, error status, instrument status, and self test. Use the ADJUST [△] and [▽] keys to select the desired status. Then press the SELECT [◁] and [▷] keys to view each item of status.

TCP/IP Status

TCP/IP status contains status information on the current IP configuration, summarized in Table 15.

Table 15: TCP/IP Status Menu

Parameter	Example Display	Description
Ethernet mac address	'Phy 00.19.b3.02.00.01'	This is the Ethernet mac address assigned to this unit at the factory.
Link status	'Connected'	Indicates if the Ethernet hardware has established a link to the network.
IP address	'IP 192.168.0.5'	The current IP address.
Subnet mask	'net 255.255.0.0'	The current subnet mask.
Default router	'rtr 192.168.0.1'	The current default gateway or router.

Error Status

The error status menu enables the user to view the number and cause of execution and parsing errors. Table 16 summarizes the error status items. See section Error Codes on page 126 for a complete list of error codes.

Table 16: Error Status Menu

Parameter	Example Display	Description
Error count	‘Error cnt 1’	Indicates the number of errors detected.
Error code	‘111 Parse Error’	Provides the error number and description of the error.

When an error is generated the front panel error LED is turned on. The ERR LED remains on until the status is interrogated, the unit is re-initialized using INIT, or the unit receives the remote command *CLS.

Instrument Status

The instrument status menu enables the user to view the instrument configuration including reports rear panel options.

Table 17: Instrument Status Menu

Parameter	Example Display	Description
Serial Number	‘Serial 001013’	Unit serial number
Version	‘Version 1.00.10A’	Firmware version
Options	‘Option 4 no’	Indicates which options, if any, are installed.

Self Test

The instrument self test runs a series of tests to check the operation of the unit. It tests communication to various peripherals on the motherboard including the GPIB chip, the PLL chips, the DDS chips, the octal DACs, the FPGA, and the serial EEPROM. If errors are encountered, they will be reported on the front-panel display when detected. The errors detected are stored in the instrument error buffer and may be accessed via the error status menu after the self test completes. See section Error Codes on page 126 for a complete list of error codes.

LOCAL

When the unit is in remote mode, the REM LED is highlighted and front-panel instrument control is disabled. Pressing the [3] (LOCAL) key re-enables local front-panel control. Note that this is technically not a secondary function in that one does not need to press [SHIFT] to activate it.

Factory Default Settings

The factory default settings are listed in Table 18. Factory default settings may be restored by power cycling the unit with the [BACK SPACE] key depressed. This forces all instrument settings except for communication parameters to the factory defaults. It is similar to the INIT secondary function and the *RST remote command, which also reset the unit to factory default settings. However the Factory Reset also performs these additional actions:

1. Resets *PSC to 1
2. Forces nonvolatile copies of *SRE and *ESE to 0.
3. Resets all stored settings from 1 to 9 back to default settings
4. Resets all stored filters to the default filter, a windowed sinc filter.
5. Resets all stored constellations to the default constellation, the QPSK constellation.
6. Erases all downloaded user waveforms and event marker files

Table 18: Factory Default Settings

Parameter	Value	Step Size
Display	Frequency	
Frequency	10 MHz	1 Hz
Phase	0 Degrees	1 Degree
Amplitude (BNC, NTYPE)	0 dBm 0.224 V_{RMS} 0.632 V_{PP}	1 dBm 0.1 V_{RMS} 0.1 V_{PP}
Offset (BNC)	0 V	0.1 V
Offset (I and Q)	0 %	0.1 %
RF PLL Filter Mode	1	
Modulation On/Off	Off	
Modulation Type	FM	
Modulation Function (AM/FM/PM)	Sine	
Modulation Function (Sweep)	Triangle	
Modulation Function (Pulse/Blank)	Square	
Modulation Function (I/Q)	PRBS	
Modulation Rate (AM/FM/PM)	1 kHz	1 kHz
Modulation Rate (Sweep)	100 Hz	10 Hz
Modulation Input Coupling	DC	
AM Depth	50 %	10 %
FM Deviation	1 kHz	1 kHz
PM Deviation	10 Degrees	10 Degrees
Sweep Deviation	1 MHz	1 MHz
AM RMS Noise Depth	10 %	10 %
FM RMS Noise Deviation	1 kHz	1 kHz
PM RMS Noise Deviation	10 Degrees	10 Degrees
Pulse/Blank Period	1000 μs	100 μs
Pulse/Blank Width	1 μs	0.1 μs
PRBS Length	9	
PRBS Period	1 μs	0.1 μs
Symbol Rate (User waveforms)	100 kHz	1 kHz

The factory default settings of the various communications interfaces are listed in Table 19. The unit may be forced to assume its factory default communication settings by power cycling the unit with the [NET(.)] key depressed.

Table 19: Factory Default Settings for Communications Parameters

Parameter	Setting
RS-232	Enabled
RS-232 Baud Rate	115200
GPIB	Enabled
GPIB Address	27
TCP/IP	Enabled
DHCP	Enabled
Auto-IP	Enabled
Static IP	Enabled
IP	0.0.0.0
Subnet Mask	0.0.0.0
Default Gateway	0.0.0.0
Bare (Raw) Socket Interface at TCP/IP port 5025	Enabled
Telnet Interface at TCP/IP port 5024	Enabled
VXI-11 Net Instrument Interface	Enabled
Ethernet Speed	100 Base-T

Analog Modulation and Sweeps

Introduction

The SG390 series generators support two types of modulation: analog modulation and vector modulation. Analog modulation refers to the modulation of a scalar parameter of the carrier signal, such as amplitude, frequency, or phase. Vector modulation refers to the modulation of the vector characteristics (amplitude and phase) of the carrier signal. Vector modulation is implemented using I/Q modulation techniques.

This chapter describes the analog modulation abilities of the SG390 series generators. The instruments are capable of AM, FM, ΦM, frequency sweeps, and pulse modulation. The modulation waveform may be an internally generated sine wave, square wave, pulse, ramp, triangle, noise, or, may be externally sourced via a rear panel BNC input. A rear panel BNC connector outputs the modulation waveform with a full scale range of ±1.00 V. The user may also download an arbitrary waveform and play it back through a user selectable filter. Finally, unlike vector modulation, analog modulation is supported at all carrier frequencies.

Configuring Analog Modulation

Five keys in the MODULATION and SELECT/ADJUST sections of the front panel are used to configure signal modulation: [ON/OFF], [MOD TYPE], [MOD FCN], [MOD RATE], and [MOD DEV]. See Figure 34.

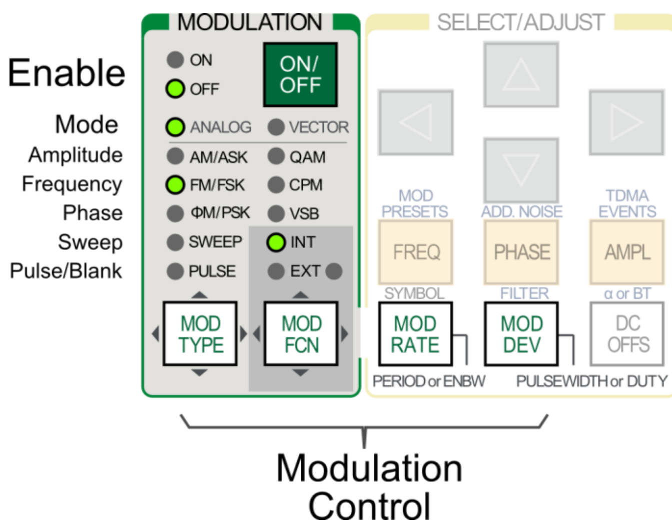


Figure 34: Front panel analog modulation control

Signal modulation is generally configured from left to right in the following order: modulation type, modulation function, modulation rate, and modulation deviation. This order of configuration is usually necessary, because the available options for configuration often depend upon previous selections.

Selecting Analog Modulation

Analog modulation is indicated when the ANALOG LED in the MODULATION section of the front panel is highlighted (see Figure 34). To configure analog modulation press [MOD TYPE] and the ADJUST [△] and [▽] keys to select the desired type of modulation: AM, FM, PM, etc. Finally, press the SELECT [◁] key, successively, until the ANALOG LED is highlighted.

MOD TYPE

Modulation Type

The [MOD TYPE] key allows the selection of which type of modulation will be applied to the synthesizer's output. The ADJUST [△] and [▽] keys are used to select the desired modulation type and the current selection is indicated with an LED. As noted above, the SELECT [◁] key must be pressed, successively, until the ANALOG LED is highlighted to ensure that analog modulation is selected. The types of analog modulation available are AM, FM, ΦM, Sweep, and Pulse.

MOD FNC

Modulation Function

The [MOD FCN] key selects one of the various functions used as the modulation waveform. The ADJUST [△] and [▽] keys are used to select the desired modulation function. The current selection will be displayed in the 7 segment display. The INT and EXT LEDs indicate whether the signal source is internal or external. If an external signal source is selected, it should be applied to the rear panel analog modulation input BNC.

Not all modulation types support all modulation functions. Table 20 shows which modulation types support which functions:

Table 20: Modulation Type vs. Function

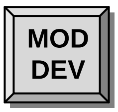
Type \ Function	Sine	Ramp	Triangle	Square	Noise	User	External
AM / FM / ΦM	✓	✓	✓	✓	✓	✓	✓
Sweep	✓	✓	✓			✓	✓
Pulse				✓	✓	✓	✓

Modulation Rate

The [MOD RATE] and [MOD DEV] keys are paired in operation and their parameters depend upon the current modulation type and function settings.

Pressing [MOD RATE] displays the modulation rate associated with the current modulation type. For the standard (AM/FM/ΦM) and sweep modulation types, this parameter is the frequency of the applied modulation waveform. The allowable range depends on both the type of modulation and the frequency selected.

For pulse modulation, this selects the period of the pulses which modulate the carrier. The pulse period is settable in 5ns increments from 1 μs to 10 s.



Modulation Deviation

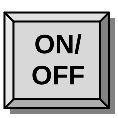
Pressing [MOD DEV] displays the deviation of the current modulation function. Depending on the modulation type, either the MOD DEV, AM DEPTH, WIDTH, or DUTY FACTOR is displayed.

For AM modulation, the AM depth is displayed. This indicates the peak percentage of the output envelope deviation. For example, if the amplitude is set to 1 V_{PP} and the AM DEPTH is set for 50%, the amplitude envelope would span from 0.5 V to 1.5 V.

For FM and sweep modulations, the deviation indicates the peak frequency excursion applied to the carrier. For example, if the carrier is set to 1.1 MHz and the deviation is set to 0.1 MHz, the carrier will span between 1 MHz and 1.2 MHz.

For ΦM modulation, the deviation indicates the peak phase excursion applied to the carrier. For example, if the deviation is set to 10°, then the carrier's phase deviation will span ±10°.

For pulse/blank modulation, the deviation indicates the pulse width or duty factor to be changed. This parameter may be either a time ("t on" for pulse or "t_off" for blank) or a duty factor. For example, for a 1 μs pulse period, a width of 500 ns or a duty factor of 50% would be equivalent, and result in the output being on for 50% of the 1 μs period.



Modulation On/Off

Finally, the [ON/OFF] key toggles the modulation on and off. The current state is indicated by the ON/OFF LEDs. Make sure that modulation is off if you want a CW (unmodulated) output from the signal generator. If the signal generator ever manifests "unexpected" behavior, check the modulation status. Modulation may have been unintentionally enabled.

Modulation Sources

The instrument's modulation capabilities include both internal and external modulation sources. The modulating waveform is replicated on the rear panel Analog Modulation Output BNC.

Linear Modulation

For AM / FM / ΦM, and Sweep, the modulation source can be either the internal generator or the rear panel external modulation input.

The internal modulation source is capable of generating sine, ramps, triangular, or square waves, at frequencies of up to 500 kHz. The instrument limits the modulation rate to 50 kHz for carrier frequencies above 62.5 MHz (93.75 MHz for the SG396).

The rear panel external modulation input supports bandwidths of 500 kHz, but the modulation bandwidth is limited to 100 kHz for f_C greater than 62.5 MHz (93.75 MHz for the SG396). The sensitivity is set such that a 1 V signal results in a full scale deviation (depth) in the output. For example: in ΦM, if the deviation is set for 10°, applying–1 V produces a –10° shift; applying 0 V produces no shift; and applying +1 V produces a +10° shift.

When modulation is enabled using an internal source, the rear panel modulation output will provide a waveform of the selected function with a full scale range of ±1 V. When external modulation is selected the modulation output tracks the applied signal.

Pulse Modulation

There are two modes of pulse modulation: pulse and blank. The mode is shown in the main display and is selected with the ADJUST [△] and [▽] keys after [MOD TYPE] is pressed.

In pulse mode, the RF signal is turned "on" by the internally generated or externally applied signal. In blank mode, the RF signal is turned "off" by the internally generated or externally applied signal.

The internal pulse modulation source is a digital waveform whose period and "on" time is settable from 1 μs to 10 s with 5 ns of adjustability. The period of the digital waveform is set via the [MOD RATE] key. The "on" time (for pulse mode) or "off" time (for blank mode) is set via the [MOD DEV] keys.

When an external input is selected the rear panel external modulation input is set for a threshold of 1V. The resulting signal is used in place of the internal source.

In pulse and blank modes, the modulation output is a 3.3 V logic signal, which tracks the pulse waveform.

Linear Noise Modulation

For AM, FM and ΦM, the noise source is pseudo random additive white Gaussian noise (AWGN). The bandwidth of the noise is set by the [MOD RATE] and the RMS deviation is set by the [MOD DEV].

The peak deviation will be about five times the set RMS deviation. This forces limits on the maximum allowed deviation corresponding to one fifth of the non-noise counterparts. For example, at a carrier frequency of 500 MHz the maximum FM deviation for a sine wave function is limited to 4 MHz, and so the maximum deviation for noise modulation is limited to 800 kHz.

For linear modulation, the rear panel output will provide 200 mV_{RMS} that will be band limited to the selected modulation rate. Again, the peak deviation will be five times this, or ±1 V_{PP}.

Pulse Noise Modulation

For pulse modulation, the noise source is a Pseudo Random Binary Sequence (PRBS). The bit period is set by the [MOD RATE]. The PRBS supports bit lengths of 2^n, for $5 \leq n \leq 32$ which correspond to a noise periodicity from 31 to 4,294,967,295 periods. The bit length n is adjusted by pressing the SELECT [◁] and [▷] keys.

During pulse PRBS modulation, the rear panel output will be a 3.3 V_{PP} waveform with a duty factor equal to $2^{n/2}$ / 2^{n-1} (approximately 50 %).

User Arbitrary Waveform Modulation

User arbitrary waveforms may be downloaded to the instrument over the remote interfaces into on board SRAM. Once downloaded the waveform may be saved into on board FLASH if desired. Waveforms stored in SRAM or FLASH may be selected as possible modulation sources from the front panel interface. Press [MOD FCN] and use the ADJUST [△] and [▽] keys to select the desired waveform. See chapter Arbitrary Waveform Generation starting on page 75 for details on creating user waveforms.

Modulation Output

A rear panel BNC provides a copy of the modulation function with ±1 V full scale range. This output will be a sine, ramp, triangle, square wave, pulse or noise depending on the selected internal modulation function.

When an external source is applied to the modulation input it will be bandwidth limited, digitized, and reproduced at the modulation output. The transfer function has a bandwidth of about 1 MHz and a latency of about 950 ns.

The modulation output is a useful source even when the RF capabilities of the instrument are not required. The sine output is exceptionally clean, with a spur-free dynamic range typically better than -80 dBc. It can be used as a pulse generator with 5 ns timing resolution, or a PRBS generator. It is a very convenient noise source, with adjustable ENBW from 1 µHz to 500 kHz.

The modulation output has a 50 Ω source impedance (to reverse terminate reflections from the user’s load) but the output should not be terminated into 50 Ω.

Amplitude Modulation

The amplitude modulation can use either the internal modulation generator or an external source. The internal modulator can generate sine, ramp, triangle, square, noise, or user waveforms.

Setting up Analog Amplitude Modulation:

MOD TYPE

Modulation Type

Press the [MOD TYPE] key and use the ADJUST [△] and [▽] keys to select AM. Press the SELECT [◁] key, successively, until the ANALOG LED in the MODULATION section of the front panel is highlighted.

MOD FNC

Modulation Function

Press the [MOD FCN] key and use the ADJUST [△] and [▽] keys to select the desired modulation function: sine, ramp, triangle, square, noise, user, or external.

MOD RATE

Modulation Rate

For internally generated modulation functions, pressing [MOD RATE] displays the modulation rate and turns on the MOD RATE LED. The value may be set using the SELECT/ADJUST arrow keys or via a numeric entry and one of the [MHz] [kHz] or [Hz] unit keys.

Internal modulation supports rates of 50 kHz for $f_c > 62.5$ MHz (93.75 MHz for the SG396) or 500 kHz for $f_c \leq 62.5$ MHz (93.75 MHz for the SG396), with 1 µHz of resolution.

External modulation supports bandwidths of 100 kHz.

MOD DEV

Modulation Depth

Press [MOD DEV] to display and set the AM modulation depth. The depth may be set using the numeric keypad and the [%] unit key, or via the SELECT/ADJUST arrow keys. The depth may range from zero to 100 % with 0.1 % resolution.

A modulation depth of *X* percent will modulate the amplitudes by $\pm X$ percent. As an example, if the amplitude is set for 224 mV_{RMS} (0 dBm), with a modulation depth of 50%, the resulting envelope would traverse 112 to 336 mV_{RMS}.

NOTE: The outputs are limited to 1 V_{RMS} (+13 dBm). If the modulation is increased such that the peak envelope would exceed this limit, the amplitude will be automatically reduced, and the screen will momentarily display “output reduced”.

ON/ OFF

Modulation On/Off

Press the [ON/OFF] key to turn the modulation on.

Amplitude Modulation Example

Figure 35 shown below is a 20 kHz carrier, with an amplitude of 1 V_{PP} into 50 Ω, amplitude modulated by an internally generated sine wave. The modulation rate is 1 kHz and the modulation depth is 100%.

Two traces are shown below. The upper trace is the 1 kHz modulation waveform from the rear panel Analog Modulation Output BNC, offset up two divisions. The lower trace is the modulated carrier (from the front panel BNC output), offset down one division.

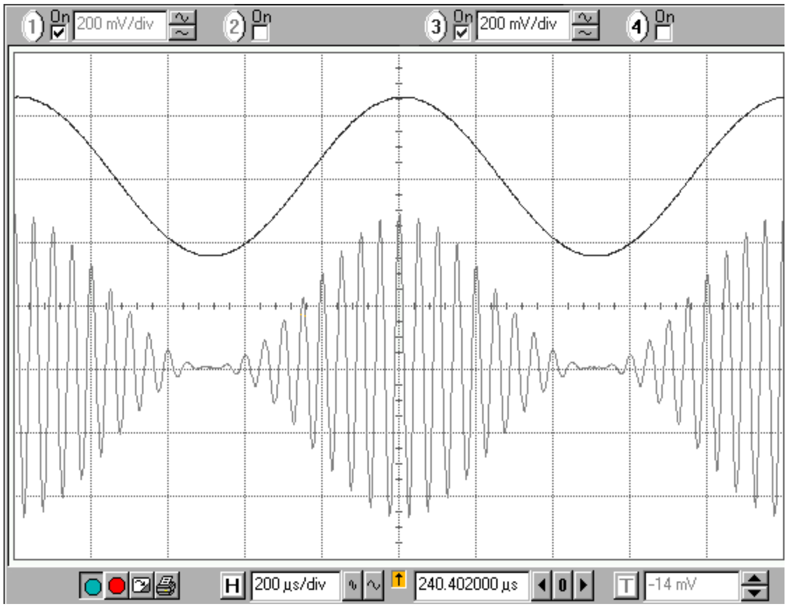


Figure 35: Amplitude modulation of a 20 kHz carrier

Frequency Modulation

The internal modulation generator or an external source may be used to modulate the frequency outputs from the front panel BNC and Type N outputs. The internal modulator can generate sine, ramp, triangle, square, noise or user waveforms.

During FM, the output frequency traverses $f_C \pm$ MOD DEV at the specified MOD RATE. For example, if the frequency is set for 1000 MHz (1 GHz), and the modulation rate and deviation are set for 10 kHz and 1 MHz, respectively, then the output will traverse from 1000 MHz, up to 1001 MHz, down to 999 MHz, and back to 1000 MHz at a rate of 10 kHz (a period of 100 µs).

The FM modulation parameters are dependent upon the frequency setting. Table 21 and Table 22 list the FM parameters as a function of frequency. All frequency bands span octaves except for the first band. The internal FM rates correspond to the upper range that the internal function generator supports. The external bandwidth is defined as the −3 dB response referenced to the external modulation source. For the bands 2 to 8, the rates and bandwidths are similar. However, the deviation increases by a factor of two, from 1 to 64 MHz, for octaves 2 through 8.

The first band has unique FM capabilities in that it allows setting the deviation of the carrier frequency to the nearest band edge. If the carrier is set on the upper edge of 62.5 MHz, the deviation is allowed to be set to 1.5 MHz (5 % of f_C). This range also supports a wider internal rate and bandwidth of 500 kHz.

For example, if the frequency is set for 100 kHz, the deviation may be set from zero to 100 kHz.

Table 21: FM Modulation vs. Frequency for SG392 and SG394

Frequency Range	Internal FM Rate. 1 µHz to:	External FM Bandwidth DC (or 4 Hz for AC) to:	FM Deviation
DC ⇔ 62.5 MHz	500 kHz	500 kHz	Smaller of f_c or 64 MHz-f_c
62.5 MHz ⇔ 126.5625 MHz	50 kHz	100 kHz	1 MHz
126.5625 MHz ⇔ 253.125 MHz	50 kHz	100 kHz	2 MHz
253.125 MHz ⇔ 506.25 MHz	50 kHz	100 kHz	4 MHz
506.25 MHz ⇔ 1.0125 GHz	50 kHz	100 kHz	8 MHz
1.0125 GHz ⇔ 2.025 GHz	50 kHz	100 kHz	16 MHz
2.025 GHz ⇔ 4.050 GHz (SG394)	50 kHz	100 kHz	32 MHz

Table 22: FM Modulation vs. Frequency for SG396

Frequency Range	Internal FM Rate. 1 µHz to:	External FM Bandwidth DC (or 4 Hz for AC) to:	FM Deviation
DC ⇔ 93.75 MHz	500 kHz	500 kHz	Smaller of f_c or 96 MHz-f_c
93.75 MHz ⇔ 189.84375 MHz	50 kHz	100 kHz	1 MHz
189.84375 MHz ⇔ 379.6875 MHz	50 kHz	100 kHz	2 MHz
379.6875 MHz ⇔ 759.375 MHz	50 kHz	100 kHz	4 MHz
759.375 MHz ⇔ 1.51875 GHz	50 kHz	100 kHz	8 MHz
1.51875 GHz ⇔ 3.0375 GHz	50 kHz	100 kHz	16 MHz
3.0375 GHz ⇔ 6.075 GHz	50 kHz	100 kHz	32 MHz

Setting up Frequency Modulation:

MOD TYPE

Modulation Type

Press the [MOD TYPE] key and use the ADJUST [△] and [▽] keys to select FM. Press the SELECT [◁] key, successively, until the ANALOG LED in the MODULATION section of the front panel is highlighted.

MOD FNC

Modulation Function

Press the [MOD FCN] key and use the ADJUST [△] and [▽] keys to select the desired modulation function: sine, ramp, triangle, square, noise, user, or external.

MOD RATE

Modulation Rate

Press [MOD RATE] to display the modulation rate. The value may be set using the SELECT/ADJUST arrow keys or via a numeric entry and one of the [MHz] [kHz] or [Hz] unit keys.

Internal modulation supports rates of 50 kHz for $f_c > 62.5$ MHz (93.75 MHz for the SG396) or 500 kHz for $f_c \leq 62.5$ MHz (93.75 MHz for the SG396), with 1 µHz of resolution.

External modulation supports bandwidths of 100 kHz.

MOD DEV

Modulation Deviation

Press [MOD DEV] to display and set the FM deviation. The deviation may be set by using the numeric keypad followed by one of the unit keys: [MHz], [kHz], or [Hz]. Alternatively, the SELECT/ADJUST arrow keys may be used.

The deviation has a range that is dependent on carrier frequency band. There are seven octaves above the lowest frequency range of DC to 62.5 MHz. The first octave (62.5 to 125 MHz) supports deviation of 1 MHz, with each succeeding octave doubling the deviation, thus achieving a 32 MHz of deviation at the 2 to 4 GHz octave.

NOTE: If the frequency is changed, the deviation may be adjusted as necessary to maintain limits imposed by the new frequency setting.

ON/ OFF

Modulation On/Off

Press the [ON/OFF] key to turn the modulation on.

Frequency Modulation Example

Figure 36 shown below is a 2 MHz carrier being frequency modulated by a 100 kHz square wave with a 1 MHz deviation. In this example of Frequency Shift Keying (FSK) the carrier frequency is being rapidly switched between 1 MHz and 3 MHz.

The top trace is from the rear panel Modulation Output BNC which shows the 100 kHz modulating waveform. The middle trace is the front panel BNC output, whose amplitude was set to 1 V_{PP}. The bottom trace is from the front panel Type N output, whose amplitude was set to 2 V_{PP}.

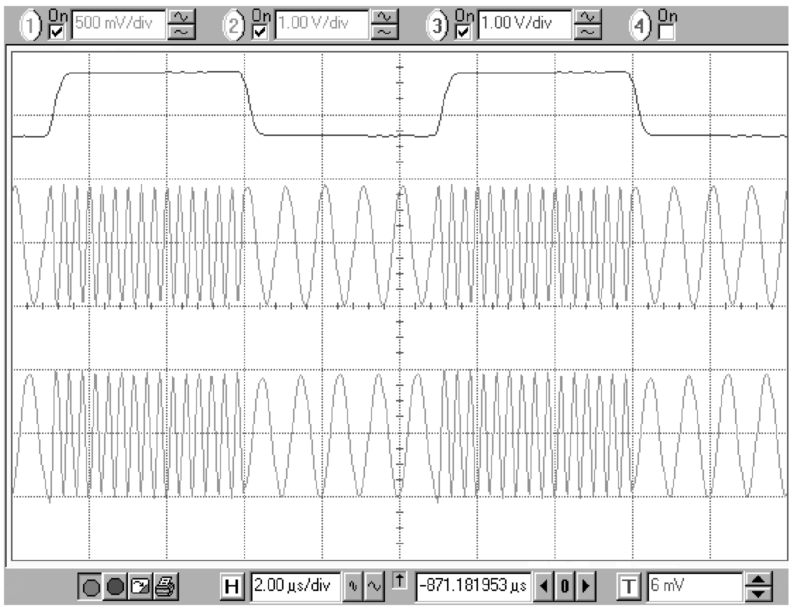


Figure 36: FSK Modulation

Phase Modulation

The phase modulation can use either the internal modulation generator or an external source. The internal modulator can generate sine, triangle, ramp, square, noise, or user waveforms.

The phase of the output traverses the specified deviation at the modulation rate. For example, with a frequency of 1000 MHz (1 GHz), and modulation rate and deviation set to 10 kHz and 45 degrees, respectively, the output will be a fixed frequency with its phase traversing ±45 degrees at a 10 kHz rate.

Setting up Phase Modulation:

MOD TYPE

Modulation Type

Press the [MOD TYPE] key and use the ADJUST [△] and [▽] keys to select ΦM. Press the SELECT [◁] key, successively, until the ANALOG LED in the MODULATION section of the front panel is highlighted.

MOD FNC

Modulation Function

Press the [MOD FCN] key and use the ADJUST [△] and [▽] keys to select the desired modulation function: sine, ramp, triangle, square, noise, user, or external.

MOD RATE

Modulation Rate

Press [MOD RATE] to display the modulation rate. The value may be set using the SELECT/ADJUST arrow keys or via the numeric keypad and one of the [MHz], [kHz], or [Hz] unit keys.

MOD DEV

Modulation Deviation

Press [MOD DEV] to display and set the ΦM deviation. The deviation may be set by using the numeric keypad and the [DEG] unit key, or via the SELECT/ADJUST arrow keys.

The phase deviation resolution depends on the frequency setting. For frequencies below 100 MHz, the phase deviation resolution is 0.01°. For frequencies between 100 MHz and 1 GHz the resolution is reduced to 0.1°, and is 1° for frequencies above 1 GHz.

For $f_c \leq 62.5$ MHz (93.75 MHz for the SG396) the accuracy of the phase deviation is 0.1 %. For $f_c > 62.5$ MHz (93.75 MHz for the SG396) the accuracy is reduced to 3 %.

ON/ OFF

Modulation On/Off

Press the [ON/OFF] key to turn the modulation on.

Phase Modulation Example

Figure 37 shown below is the frequency spectrum of a 0 dBm, 50 MHz carrier, being phase modulated by a 10 kHz sine with a deviation of 137.78°. Here, the modulation index, β = phase deviation = 137.78° × 2π / 360° = 2.40477 radians. For phase modulation by a sine, the carrier amplitude is proportional to the Bessel function $J_0(\beta)$, which has its first zero at 2.40477, which suppresses the carrier to below -88 dB.

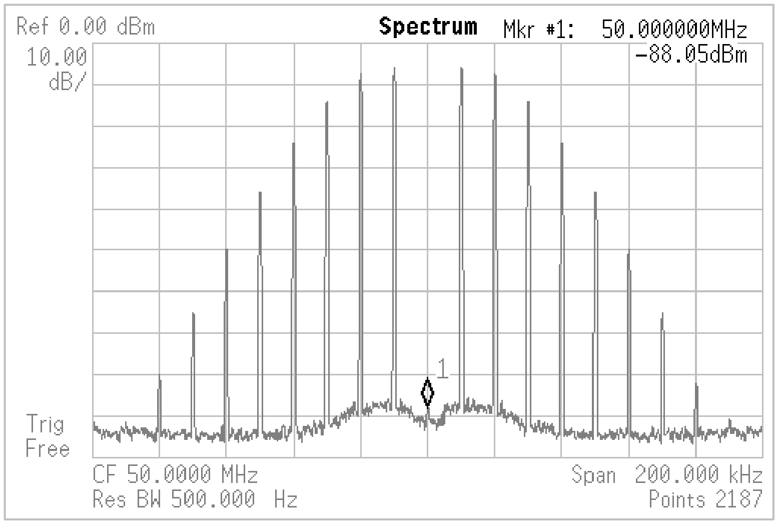


Figure 37: Spectrum of Phase Modulated 50 MHz Carrier

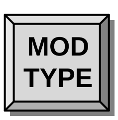
Pulse and Blank Modulation

Pulse modulation includes both pulse and blank modulation of the front panel BNC and Type N outputs. Pulse and blank modulation are logical complements of each other—pulse modulation enables the output when the pulse waveform is “true”, while blank modulation disables the output. The functions supported are square, noise (Pseudo Random Binary Sequence — PRBS), user, and external.

For internal square wave function the instrument has a 32-bit timing generator clocked by a 200 MHz source. This allows the period to be set from 1 μs to 10 s with 5 ns resolution. The pulse duration can then be set from 100 ns up to the full period (less 100 ns). The internal generated pulse waveform is available at the rear panel Modulation Output BNC.

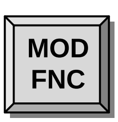
For pulse (blank) modulation, the output is turned on (off) when the source is at logic high.

Setting up Pulse Modulation:



Modulation Type

Press the [MOD TYPE] key and use the ADJUST [△] and [▽] keys to select pulse or blank modulation.

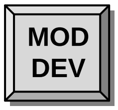


Modulation Function

Press the [MOD FCN] key and use the ADJUST [△] and [▽] keys to select the desired modulation function: pulse, noise, user, or external. If external, then CMOS logic levels applied to the rear panel modulation input control the pulse or blanking of the outputs.

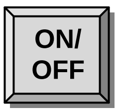
Pulse Period

Press [MOD RATE] to display the pulse modulation period for the internal source. The period may be set by using the numeric keypad followed by one of the unit keys: [ns], [µs], or [ms]. Alternatively, the SELECT/ADJUST arrow keys may be used. The period may be set with 5 ns resolution.



Pulse Width or Duty Factor

Press [MOD DEV] to display and set the pulse width or duty factor of the internal source. The value may be set using numeric keypad followed by one of the unit keys: [ns], [µs], or [ms] (for pulse width) or [%] (for duty factor).



Modulation On/Off

Press the [ON/OFF] key to turn the modulation on.

Pulse Modulation Example

Figure 38 shows the front panel BNC and Type N outputs for a pulse modulated carrier frequency of 50 MHz. The internal pulse modulator was set to 1 µs period, with a 300 ns pulse width (or a 30% duty cycle).

The output amplitudes were set to 2 V_{PP} into 50 Ω. The top trace is the rear panel Modulation Output signal. The middle trace is the BNC output. The bottom trace is the Type N output. Both traces show about 50 ns latency in their response to the gating signal. The Type N output also shows some gate feed-though at the leading edge if the signal.

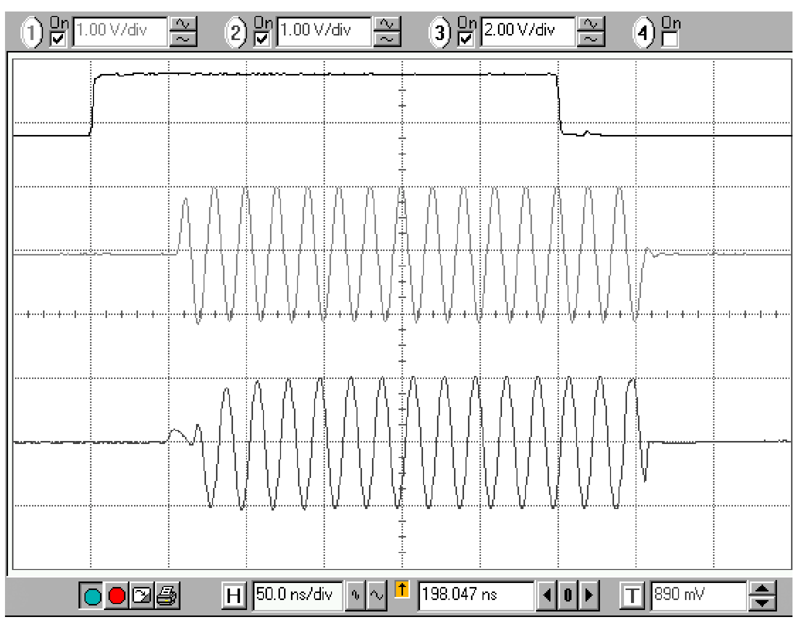


Figure 38: Pulse modulated 50 MHz carrier

Phase Continuous Frequency Sweeps

Frequency sweeps allow the traversing of an entire frequency band. The sweep modulation function may be sine, triangle, ramp, user or an external source. Sweep rates of up to 120 Hz and sweep ranges from 10 Hz up to an entire frequency band are supported with resolutions of 1 μHz.

Frequency sweeps can require the instrument's RF VCO to sweep through an entire octave. For the sweep to be phase continuous the RF VCO PLL must remain in "LOCK" during the sweep. This is why the maximum sweep rate is limited to 120 Hz and why the frequency slew rate is internally limited for the ramp function. The slew rate of external modulation sources should also be limited if a phase continuous sweep is required.

The RF Synthesizers have eight frequency bands as shown in Tables below:

Table 23: Sweep Frequency Bands for the SG392 and SG394

Band	Frequency
1	DC ⇒ 64 MHz
2	59.375 ⇒ 128.125 MHz
3	118.75 ⇒ 256.25 MHz
4	237.5 ⇒ 512.5 MHz
5	475 ⇒ 1025 MHz
6	950 ⇒ 2050 MHz
7 (SG394)	1900 ⇒ 4100 MHz

Table 24: Sweep Frequency Bands for the SG396

Band	Frequency
1	DC ⇒ 96 MHz
2	89.0625 ⇒ 192.1875 MHz
3	178.125 ⇒ 384.375 MHz
4	356.25 ⇒ 768.75 MHz
5	712.5 ⇒ 1537.5 MHz
6	1425 ⇒ 3075 MHz
7	2850 ⇒ 6150 MHz

Setting up Frequency Sweeps:

MOD TYPE

Modulation Type

Press the [MOD TYPE] key and use the ADJUST [△] and [▽] keys to select sweep modulation.

MOD FNC

Modulation Function

Press the [MOD FCN] key and use the ADJUST [△] and [▽] keys to select the desired modulation function: sine, ramp, triangle, user, or external.

MOD RATE

Sweep Rate

Press [MOD RATE] to display the modulation rate. This value may be set using the SELECT/ADJUST arrow keys or via numeric keypad followed by a unit key. The rate may be set from 1 μHz to 120 Hz with a resolution of 1 μHz.

MOD DEV

Sweep Deviation

Press [MOD DEV] to display and set to the sweep deviation. The value may be set using numeric keypad followed by a unit key, or via the SELECT/ADJUST arrow keys. The deviation may be set to sweep an entire band or any part thereof. Refer to Table 23 and Table 24 for details on frequency band limits.

ON/ OFF

Modulation On/Off

Press the [ON/OFF] key to turn the modulation on.

Vector Modulation

Introduction

The SG390 series generators support two types of modulation: analog modulation and vector modulation. Analog modulation refers to the modulation of a scalar parameter of the carrier signal, such as amplitude, frequency, or phase. Vector modulation refers to the modulation of the vector characteristics (amplitude and phase) of the carrier signal. Vector modulation is implemented using In-phase/Quadrature (I/Q) modulation techniques.

This chapter describes the vector modulation abilities of the SG390 series generators. The SG390 series includes standard support for I/Q modulation on RF carriers between 400 MHz and 6.075 GHz. In addition, they feature a dual, arbitrary waveform generator operating at 125MHz for baseband signal generation. The generator has built-in support for the most common vector modulation schemes: ASK, QPSK, DQPSK, π/4 DQPSK, 8PSK, FSK, CPM. QAM (4 to 256), 8VSB, and 16VSB. It also includes built-in support for all the standard pulse shaping filters used in digital communications: raised cosine, root-raised cosine, Gaussian, rectangular, triangular, and more. Lastly, it provides direct support for the controlled injection of additive white Gaussian noise (AWGN) into the signal path.

The baseband generator supports the playback of pure digital data. It automatically maps digital symbols into a selected IQ constellation at symbol rates of up to 6 MHz and passes the result through the selected pulse shaping filter to generate a final waveform updated in real time at 125 MHz. This baseband signal is then modulated onto an RF carrier using standard IQ modulation techniques.

This architecture leads to a greatly simplified and productive user experience. PRBS data and simple patterns can be played back directly from the front panel. Trade-offs in filter bandwidth versus power efficiency can be explored from the front panel in real time without the need to download complex new waveforms each time. Likewise, the degradation of a signal by additive white Gaussian noise (AWGN) can be easily manipulated from the front panel.

Although not directly configurable from the front panel, the SG390 series generators also support the generation of time domain, multiple access (TDMA) signals and event markers. Event markers enable the user to mark events during the playback of a waveform, such as the start of a frame, or a slot within a frame. Three rear-panel BNC outputs tied to these events may be programmed to pulse high or low for an arbitrary number of symbols in order to synchronize other instrumentation with the event. Any one of these event markers may be selected to control the RF power of the output, thereby creating an RF burst useful for implementing TDMA signals. The RF burst follows a raised cosine profile with a ramp rate that can be configured to be 1, 2, 4, or 8 symbols wide.

Naturally, the SG390 series instruments can be extended by the user if desired by downloading and storing up to ten custom constellations, filters, and waveforms each. Complex constellations involving rotating coordinate systems, or differential encoding are supported directly. Filters with up to 24 symbols of memory are supported. 2MB of flash is available for waveform storage and playback. Due to the fact that the SG390 performs the symbol mapping and pulse shaping in real time, this is enough space to store 2 MSym of QAM 256 data or 16 MSym of 1 bit FSK data. For a 3-bit GSM-EDGE waveform running at 270.833 kSym/s this is enough storage for over 20 seconds of playback data which is updated at 125 MHz. Playing back such a waveform using raw 16-bit values for I and Q at 125 MHz would require more than 9 GB of storage.

SG390 series generators come with a number of modulation presets for demonstrating the various modulation capabilities of the instrument. Sample modulation waveforms and setups are included for communications standards such as NADC, PDC, DECT, APCO Project 25, TETRA, GSM, GSM-EDGE, and W-CDMA.

Finally, the rear panel BNC I-Q modulation inputs and outputs enable arbitrary vector modulation via an external source. The external signal path supports 300 MHz of RF bandwidth with a full scale range of ±0.5 V and a 50 Ω input impedance.

A Primer on Digital Communications

Communications refers to the transmission of information from one entity to another. The information may be a person’s voice, a picture, or written text. For two people in the same room, communication is very natural. They can speak directly to each other, point to a printed picture, or exchange books for reading. In many cases, however, it is desirable to communicate with people who are very far away, for which direct communication is impossible. In this case, one needs a different medium to enable communication.

In the pre-industrialized world, people learned to communicate over moderate distances using flags or smoke signals. In today’s world, however, long distance communication is accomplished by encoding information onto an electrical signal, which can be transmitted over very long distances at close to the speed of light. The electrical signal is usually an RF carrier and the information is encoded by modulating or altering the carrier in some way. The modulations are usually one of three types: amplitude, frequency, or phase.

In most cases, the information being transmitted is an analog signal. The acoustic vibrations from a person’s voice, for instance, can be converted into an electrical signal with the use of a microphone. The resulting electrical signal is an analog signal, which may be easily converted back into voice with an amplifier and a speaker. In traditional analog communications, the analog signal itself is used to modulate the RF directly. In FM radio, for example, the amplified analog voice signal from the microphone is used to modulate the frequency of the RF carrier directly. The primary advantage of such a scheme is its simplicity and affordability. Receivers were fairly easy to design and cheap to produce. The disadvantage of analog communication is that it is wasteful of power and bandwidth, and susceptible to degradation by noise.

Digital communications refers to the transmission of digital data or numbers, instead of analog signals. Analog signals can be converted into digital data with the use of an analog to digital converter (ADC). The ADC measures the analog signal at an instant in time and assigns a number to it. Big signals are assigned big numbers and small signals are assigned small numbers. The ADC samples the size of the analog signal every few microseconds and assigns a number proportional to the size of the signal at each instant. In this way, an analog signal is ultimately converted into a sequence of numbers.

Digital data may then be converted back into analog signals with the use of a digital to analog converter (DAC). A DAC takes a number and converts it into a voltage proportional to the number—small numbers produce small voltages, and large numbers produce large voltages. By updating the number in the DAC every few microseconds with the sequence of numbers produced by the ADC, the original analog signal may be reproduced.

Constellations

One important characteristic of digital signals that distinguishes them from analog signals is that they are quantized and bounded. Normally, digital signals are represented as binary sequences of finite length. A 1-bit (binary) signal has only two states: 0 or 1. A 2-bit signal is represented with two binary digits in sequence and, thus, has 4 states: 00, 01, 10, and 11. A 3-bit signal will have 8 states. An N-bit signal will have 2^N states.

The transmission of digital data is straight forward. Like analog communication, information is encoded in a modulation of the amplitude, frequency, or phase of an RF carrier. However, unlike analog communications, only a finite number of modulated states are allowed. In binary phase shift key (BPSK) modulation, for example, only two phases are allowed. These are usually chosen to be 0 and 180°. One phase represents a 0 and the other represents a 1. Similarly, in quadrature phase shift key (QPSK) modulation, only 4 phases are allowed. These are usually chosen to be ±45° and ±135°. Each of the four phases is associated with a unique 2-bit binary sequence: 00, 01, 10 or 11.

The set of allowed phases and their mapping to binary sequences constitutes a digital constellation. The constellation may be succinctly represented in a polar diagram of the I/Q plane identifying the allowed states and their mapping. See Figure 39.

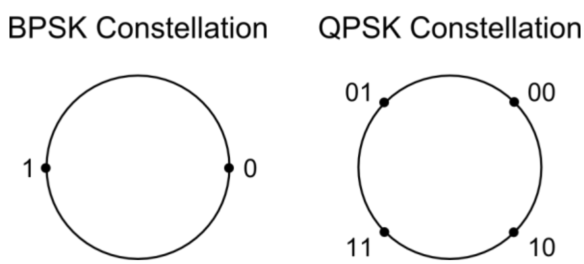


Figure 39: Example modulation constellations for BPSK and QPSK.

A vector signal generator can modulate both the amplitude and the phase of an RF carrier, simultaneously. This enables many more options for defining symbol constellations. In quadrature amplitude modulation (QAM), both the amplitude and phase of the allowed states are defined, usually in a rectangular array as shown in Figure 40.

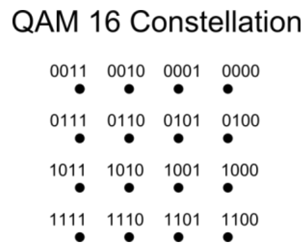


Figure 40: Example QAM constellation.

Gray Code

It is important to recognize that the mapping from symbol to constellation point is completely arbitrary and at the discretion of the communications protocol designer. Usually, some form of Gray coding is utilized in order to minimize the possible transmission of multi-bit errors. A Gray code mapping has the property that all nearest neighbor constellation points differ in code by at most 1 bit. The example QPSK constellation in Figure 39 satisfies this property, but the example QAM 16 constellation in Figure 40 does not. For the QPSK constellation, the nearest neighbors to 00 are 01 and 10. Both of these transitions involve a single bit transition. This property holds true for all the QPSK constellation points. In contrast, point 0001 in the QAM 16 constellation, of Figure 40 includes the nearest neighbor point 0010, which involves two simultaneous bit transitions, violating the basic property of Gray codes.

Gray code helps to reduce the accidental transmission of multi-bit errors, thereby increasing the effectiveness of any error correction measures included in the communications protocol. Unfortunately, Gray code mappings are not unique. Nor is there any agreement on a standard mapping. Each protocol includes its own unique Gray code mapping. As such the SG390 series generators use the simple mapping scheme shown in the examples and leave it to the user to encode their data to match the mapping scheme of the protocol they are using.

Susceptibility to Noise

As mentioned earlier, digital constellations have a finite number of allowed states. A BPSK constellation, for instance, has only two allowed states: 0° and 180°. This property greatly enhances the robustness of digital communications in the face of noise. Since a BPSK constellation contains only two allowed states, any transmission which includes a deviation from these two states must be the result of noise. If the noise deviations are small, the receiver can recover the actual transmission with 100 % accuracy by assuming the nearest allowed constellation point was the intended transmission. This is in stark contrast to analog communications, where any noise in the bandwidth of the channel will degrade the fidelity of the transmitted signal. Digital transmissions suffer no degradation until the noise becomes so great that the nearest neighbor principle is not always true. Even then, errors can often be corrected by the receiver if the protocol makes use of Gray code and sufficient redundancy has been built into the transmission.

Pulse Shaping Filters

Up to now, we have emphasized the fact that digital constellations have a finite number of allowed states, but we have not discussed how the signal transitions from one allowed state to the next. The simplest method would be to jump as quickly as possible from state to state. Although simple, this method turns out to be undesirable in most cases, because it creates spurious energy at large offsets from carrier. This is important because the RF spectrum is a limited resource that has to be shared by many people cooperatively at the same time. Lots of people are trying to transmit data simultaneously. Without cooperation, all these transmissions would interfere with one another and nobody would be able to communicate.

One of the most common means of sharing the RF spectrum is with frequency division multiple access (FDMA). In this scheme the RF spectrum is divided into many small frequency bands. Each user is assigned one band and may transmit at will as long as their transmission is confined to their assigned band. If this basic rule is obeyed, everyone can communicate simultaneously without interference. Unfortunately transmissions which jump from symbol to symbol as quickly as possible invariably violate this rule. Thus, almost all communication protocols stipulate pulse shaping filters to overcome this problem.

Pulse shaping filters limit the bandwidth of a digital transmission by converting the sharp transitions into gradual transitions with much lower bandwidth. They are essentially low pass filters, which filter out all the high frequency components of the sharp transitions.

Intersymbol Interference

Pulse shaping filters fix the frequency domain problems by filtering out the high frequency components that would interfere with neighboring users. Unfortunately, they introduce a new problem in the time domain, intersymbol interference (ISI). The problem can be understood by observing the impulse response of the pulse shaping filter as a function of time. Generally speaking, pulse shaping filters with low bandwidth have long response times. Conversely, filters with relatively high bandwidth have short response times. Low bandwidth is good, but long response times create a problem.

A digital communications receiver must make a decision about which symbol was transmitted after every symbol period. The decision is usually made when the impulse response for that symbol is at its peak. Intersymbol interference occurs when the response of adjacent symbols interferes with the response of the current symbol at the moment the decision is made.

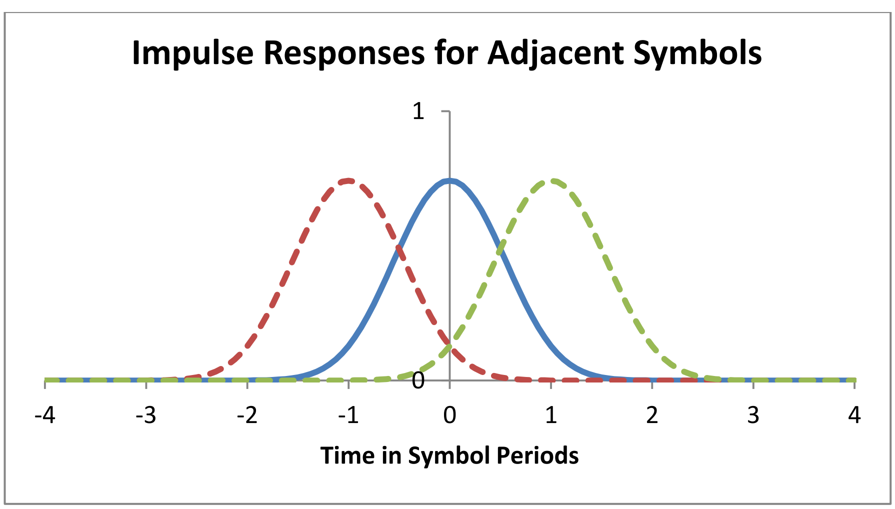


Figure 41: Impulse responses showing intersymbol interference.

Figure 41 shows the impulse responses of three symbols superimposed on each other. At time t = 0, the receiver must decide which symbol was transmitted. Notice that the responses from both the previous symbol and succeeding symbols are nonzero. The full response at time t = 0 is the superposition of all three responses. The residual responses of the adjacent symbols will add or subtract to the symbol under question, thus, interfering with the decision about what was transmitted.

Common Filters

Three different pulse shaping filters are commonly used in digital communications: the raised cosine filter, the root-raised cosine filter, and the Gaussian filter. Each addresses the problem of ISI differently.

Raised Cosine Filter

The first strategy for dealing with ISI is to remove it with a cleverly designed filter that has zero intersymbol interference. The raised cosine filter meets this criterion. It is defined by the following frequency response:

$$H(f) = \begin{cases} T, & |f| \le \frac{1-\alpha}{2T} \\ \frac{T}{2}\left[1+\cos\left(\frac{\pi T}{\alpha}\left[|f| - \frac{1-\alpha}{2T}\right]\right)\right], & \frac{1-\alpha}{2T} < |f| < \frac{1+\alpha}{2T} \\ 0, & |f| \ge \frac{1+\alpha}{2T} \end{cases}$$

where f is the frequency, T is the symbol period and α is a dimensionless parameter controlling the excess bandwidth of the filter. When α = 0, the filter approximates a brick wall. When α = 1.0 the filter has 100 % excess bandwidth over the brick wall filter, i.e. it is twice as wide.

The impulse response of the raised cosine filter is given by

$$h(t) = sinc\left(\frac{t}{T}\right)\frac{cos\left(\frac{\pi\alpha t}{T}\right)}{1-\frac{4\alpha^2 t^2}{T^2}}$$

where sinc(x) = sin(πx)/(πx). Figure 42 shows the impulse response of the raised cosine filter for α = 1.0, α = 0.5, and α = 0.3. Notice that as α is reduced the impulse response lasts longer and extends over many symbols. Normally, this behavior would cause intersymbol interference. However, the sinc(x) function in the impulse response of the raised cosine filter has the important property that it goes to zero at all integer values of x except 0 where it is 1.0. This is what leads to zero intersymbol interference. A plot showing the impulse response of adjacent symbols should make this clear.

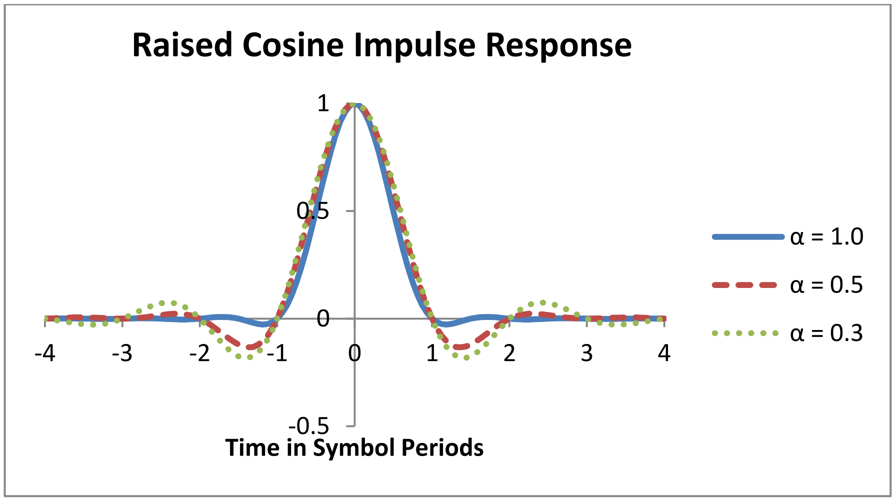


Figure 42: Raised cosine impulse response.

Figure 43 shows the impulse responses of adjacent symbols for a raised cosine filter with α = 0.3. Notice that the impulse responses of all adjacent symbols goes to zero at t = 0 when the receiver makes its decision. Thus, even though the full response lasts for about 8 symbol periods, the response of neighboring symbols is always zero at the moment a decision is being made.

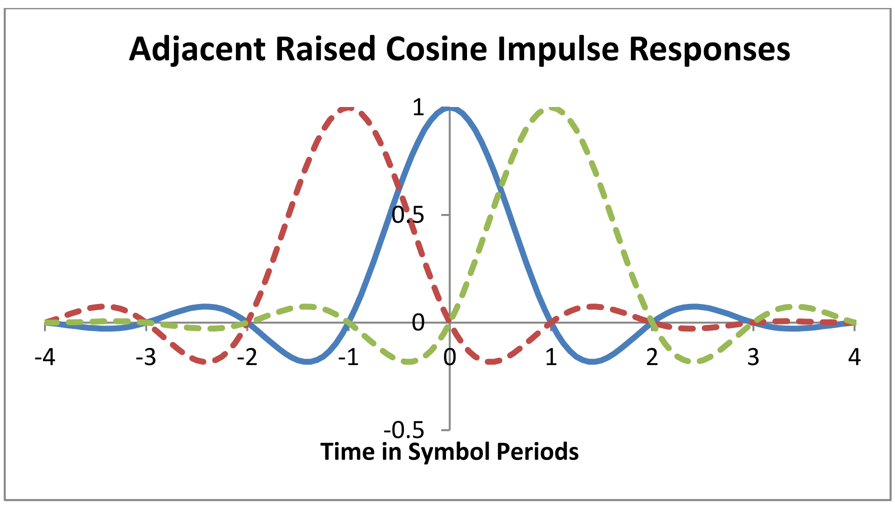


Figure 43: Raised cosine (α = 0.3) impulse responses showing zero ISI.

Root-Raised Cosine Filter

The root-raised cosine filter is perhaps the most common pulse shaping filter. Its frequency response is given by the square root of the raised cosine filter.

$$H_{root}(f) = \sqrt{|H(f)|}$$

The impulse response of the root-raised cosine filter is given by

$$h(t) = \frac{\sin\left[\pi\frac{t}{T}(1-\alpha)\right] + 4\alpha\frac{t}{T}\cos\left[\pi\frac{t}{T}(1+\alpha)\right]}{\pi\frac{t}{T}\left[1-\left(\frac{4\alpha t}{T}\right)^2\right]}$$

where all parameters have the same definitions as in the raised cosine filter.

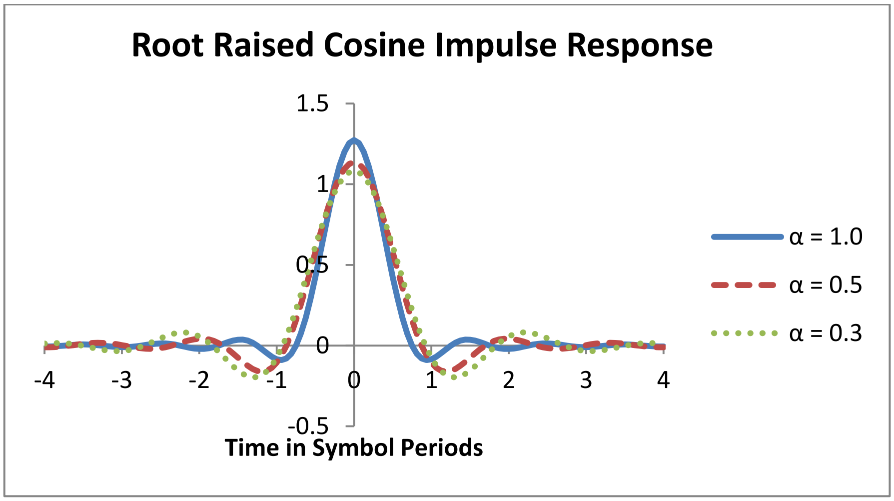


Figure 44: Root-raised cosine impulse response.

Figure 44 shows the impulse response of the root-raised cosine filter for α = 1.0, α = 0.5, and α = 0.3. The response is qualitatively similar to the raised cosine response, but it does not generally have zero ISI. However, cascading two such filters together creates a raised cosine filter which does have zero ISI. Thus, many communication protocols stipulate that both the transmitter and the receiver use root-raised cosine filters. The transmitter's filter limits the bandwidth of the transmitted waveform to prevent adjacent channel interference. The receiver's filter improves signal recovery by further filtering out noise in the communication's channel. Finally, the two filters in combination produce a raised cosine response which does have zero ISI.

Gaussian Filter

The last strategy for dealing with intersymbol interference is to accept it, but limit its reach to just the nearest neighboring symbols in time. The Gaussian filter is a common choice here because it has no ringing, a short duration, and relatively compact bandwidth. It is created by convolving a rectangular filter with a Gaussian.

$$h(t) = g(t) * rect\left(\frac{t}{T}\right)$$

where T is the symbol period, g(t) is a Gaussian, and *rect*(t/T) is defined by

$$rect\left(\frac{t}{T}\right) = \begin{cases} \frac{1}{T}, & |t| < \frac{T}{2} \\ 0, & \text{otherwise} \end{cases}$$

The Gaussian *g*(t) is given by

$$g(t) = \frac{\exp\left(\frac{-t^2}{2\delta^2 T^2}\right)}{\sqrt{2\pi} \cdot \delta T}$$

with

$$\delta = \frac{\sqrt{\ln(2)}}{2\pi BT}$$

BT is the 3 dB bandwidth-symbol time product, a dimensionless factor similar to α in raised cosine filters that controls the bandwidth of the filter.

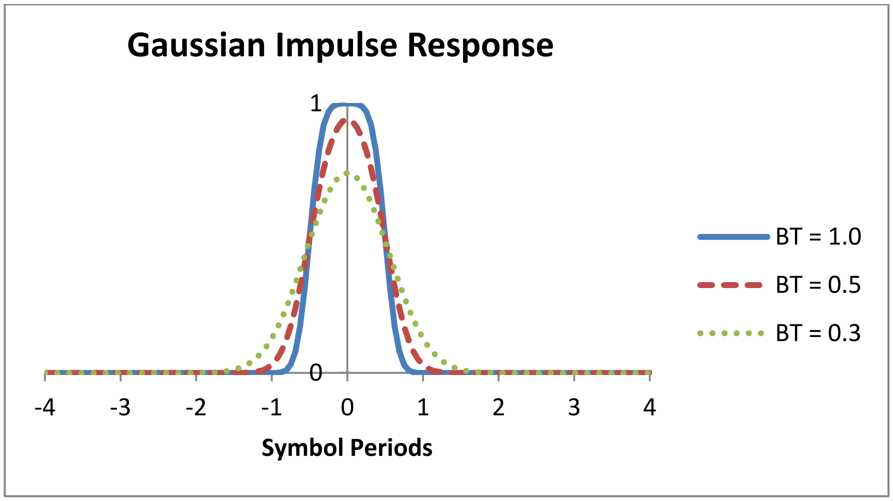


Figure 45: Gaussian impulse response.

Figure 45 shows the impulse response of the Gaussian filter for BT = 1.0, BT = 0.5, and BT = 0.3. Intersymbol interference is limited to the nearest neighbor symbols which simplifies receiver design.

Error Vector Magnitude

As noted above, digital communication protocols often stipulate both a symbol constellation and a pulse shaping filter. Given a constellation, a pulse shaping filter, and a set of symbols to transmit, one can map out the expected trajectory of the modulated RF carrier as a function of time as each symbol is transmitted. The trajectory can be characterized by a vector quantity which identifies the amplitude and phase of the RF at a given moment in time. One can then evaluate the quality of a digital transmission by comparing the received trajectory with the expected reference trajectory. The deviation between the two is a vector quantity indicating the error of the received signal at a given moment in time. The magnitude of the error is called the error vector magnitude (EVM). Figure 46 diagrams the relationship on the IQ plane. The measured signal is compared to the reference signal and the difference is given by the error vector. The length of the error vector is the error vector magnitude.

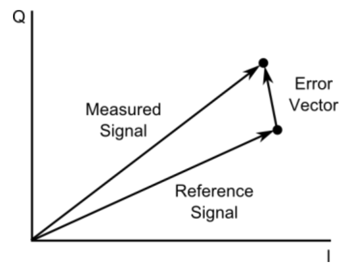


Figure 46: Error vector magnitude is the length of the error vector.

The error vector magnitude is often reported as a percentage relative to some standard signal, such as the magnitude of a constellation point.

Error vectors are helpful in characterizing the quality of a transmitted signal. They are a natural measure of the noise in a communications channel, but they can also help identify defects of a transmitter, such as amplifier compression or an IQ gain imbalance.

Vector Modulation Configuration

The SG390 series generators have broad support for all the standard types of vector modulation used in digital communications. However, the architecture of the instruments differs from those of many other generators on the market. An understanding of this architecture, therefore, is helpful in configuring them.

Architecture

The SG390 series generators include baseband dual arbitrary waveform generators for use with a built-in I/Q modulator in the creation of digital communication waveforms. The basic architecture of the baseband generator is diagrammed in Figure 47.

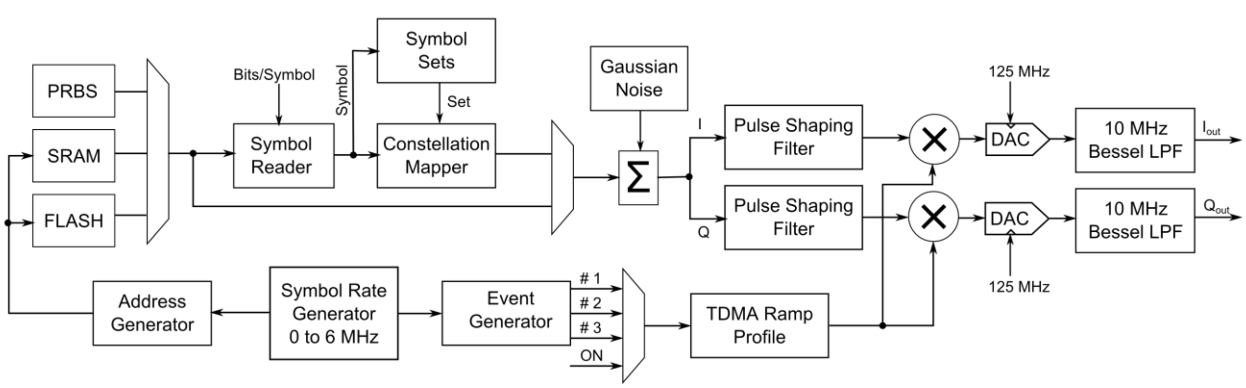


Figure 47: The SG396 arbitrary waveform generator

Symbols are read out of memory or generated by a PRBS engine at rates of up to 6 MHz. They are then optionally mapped into constellation points. If desired, the constellation points may be degraded by additive white Gaussian noise (AWGN) before being passed through dual pulse shaping filters—one for I and one for Q. The outputs of the filters are gated by a TDMA ramp profile controlled by the event generator. The results are sent to 14-bit, high-speed DACs running at 125 MHz. The final result is passed through an analog Bessel filter before being combined with the RF at the front panel.

The important point to realize is that the symbol constellation mapping, the noise generation, and the pulse shaping filters are integrated blocks within the generators that are distinguishable from the waveform itself and can be independently configured. Changing the pulse shaping filters does not involve a new waveform download because they are independent blocks within the generator. The same waveform can be played back with different pulse shaping filters by merely selecting a different filter from the front panel.

The built-in symbol constellation mapping is very flexible. It can easily support static as well as rotating constellations with differential encoding. This feature greatly reduces the storage requirements for waveforms, because pure 1-bit or 2-bit digital symbols may be stored rather than 16-bit I and Q constellation points, leading to a factor of 32 in potential storage savings.

Furthermore, when the storage savings from the symbol mapping are combined with the savings from on the fly pulse shape filtering the savings can be dramatic. For the GSM EDGE example mentioned in the introduction, the difference is almost a factor of 5,000.

Front Panel Configuration

Five keys in the MODULATION and SELECT/ADJUST sections of the front panel are used to configure vector signal modulation: [ON/OFF], [MOD TYPE], [MOD FCN], [MOD RATE], and [MOD DEV]. See Figure 48.

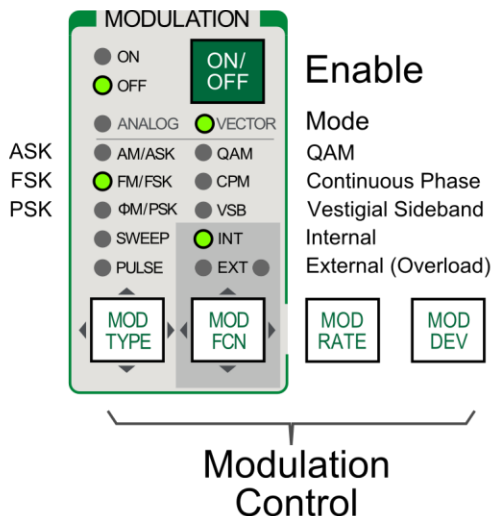
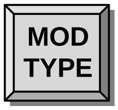


Figure 48: Front panel vector modulation control.

Signal modulation is generally configured from left to right in the following order: modulation type, modulation function, modulation rate, modulation deviation, and pulse shaping filter. This order of configuration is usually necessary, because the available options for configuration often depend upon previous selections.

Selecting Vector Modulation

Vector modulation is indicated when the VECTOR LED in the MODULATION section of the front panel is highlighted (see Figure 48). To configure vector modulation press [MOD TYPE] and the ADJUST [△] and [▽] keys to select the desired type of modulation: ASK, FSK, PSK, etc. Finally, press the SELECT [◁] and [▷] keys until the VECTOR LED is highlighted with the desired type of modulation.

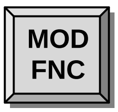


Modulation Type

The [MOD TYPE] key allows the selection of which type of modulation will be applied to the synthesizer's output. The ADJUST [△] and [▽] keys are used to select the desired modulation type: ASK, FSK, PSK, QAM, CPM, or VSB. The current selection is indicated with an LED.

Modulation Subtype

With modulation type displayed, press the SELECT [◁] and [▷] keys until the VECTOR LED is highlighted with the desired subtype of modulation: vector function, 1-bit, 2-bit, etc. The modulation subtype determines the bits per symbol and the constellation pattern used in the modulation. The function subtype indicates that the constellation mapping mechanism is bypassed and that symbols read from memory are passed directly to the pulse shaping filters. All other vector subtypes are associated with a constellation into which symbols of the defined width get mapped.



Modulation Function

The [MOD FCN] key selects one of the various functions used as the modulation waveform. The ADJUST [△] and [▽] keys are used to select the desired modulation function. The current selection will be displayed in the 7 segment display. The INT and EXT LEDs indicate whether the signal source is internal or external. If an external signal source is selected, it should be applied to the rear panel vector modulation input BNCs.

The modulation functions available for the vector function subtype are similar to those offered for analog modulation: sine, ramp, triangle, square, noise, user, and external. For the digital modulation subtypes, the available waveforms include: PRBS data, pattern data, and user data.

Simple Waveforms

For the vector function subtype, the SG390 series generators offer several simple waveforms similar to those available for analog modulation: sine, ramp, triangle, square, and noise.

PRBS Data

The SG390 series generators can generate pseudo random binary sequences (PRBS) for use with digital modulation subtypes. To select a PRBS waveform press [MOD FCN] and then the ADJUST [△] and [▽] keys until “Func PRBS” is selected in the 7 segment display. The length of the PRBS waveform may be adjusted from 5 to 32 with the SELECT [◁] and [▷] keys. The default PRBS length is 9. The PRBS patterns are generated with linear feedback shift registers. Table 25 shows the generating polynomials for each PRBS pattern. The output of the PRBS generator is inverted so that the all-ones state is excluded, rather than the all-zeros state. All PRBS waveforms start in the all-zeros state.

Table 25: PRBS generating polynomials

Length	Polynomial	Length	Polynomial
5	$x^5 + x^3 + 1$	19	$x^{19} + x^{18} + x^{10} + x^2 +1$
6	$x^6 + x^5 + 1$	20	$x^{20} + x^{17} + 1$
7	$x^7 + x^6 + 1$	21	$x^{21} + x^{19} + 1$
8	$x^8 + x^7 + x^5 + x^3 +1$	22	$x^{22} + x^{21} + 1$
9	$x^9 + x^5 + 1$	23	$x^{23} + x^{18} + 1$
10	$x^{10} + x^7 + 1$	24	$x^{24} + x^{23} + x^{18} + x^{14} +1$
11	$x^{11} + x^9 + 1$	25	$x^{25} + x^{22} + 1$
12	$x^{12} + x^{11} + x^8 + x^6 +1$	26	$x^{26} + x^{25} + x^{16} + x^5 +1$
13	$x^{13} + x^{12} + x^8 + x^2 +1$	27	$x^{27} + x^{26} + x^{16} + x^2 +1$
14	$x^{14} + x^{13} + x^8 + x^6 +1$	28	$x^{28} + x^{25} + 1$
15	$x^{15} + x^{14} + 1$	20	$x^{29} + x^{27} + 1$
16	$x^{16} + x^{15} + x^9 + x^6 +1$	30	$x^{30} + x^{29} + x^{16} + x^4 +1$
17	$x^{17} + x^{14} + 1$	31	$x^{31} + x^{28} + 1$
18	$x^{18} + x^{11} + 1$	32	$x^{32} + x^{31} + x^{18} + x^{10} +1$

Pattern Data

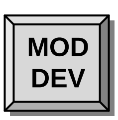
Digital modulation subtypes may also be modulated with 16-bit patterns. To select a pattern waveform from the front panel, press [MOD FCN] and then the ADJUST [△] and [▽] keys until “Func Pattern” is selected in the 7 segment display. The current pattern is shown is the 7 segment display as hexadecimal digits. Once selected, the pattern may be edited from the front panel by pressing the SELECT [◁] and [▷] keys and ADJUST [△] and [▽] keys to modify each hexadecimal digit. Press [ENTER] to update settings with the new pattern. The default pattern is the binary sequence 01010101 01010101, which corresponds to the hexadecimal value 0x5555.

User Data

User data may be downloaded into on-board SRAM and subsequently saved into FLASH. If user waveforms are available for the selected modulation subtype, they may be selected as a modulation function. With modulation function displayed, and an appropriate digital modulation format selected, press the ADJUST [△] and [▽] keys until the desired user waveform is selected.

Modulation Rate

Pressing [MOD RATE] displays the modulation rate associated with the current modulation type. For digital modulation subtypes, this is the symbol rate, otherwise, it is the frequency or bandwidth of the selected waveform.



Modulation Deviation (Scale Factor)

Pressing [MOD DEV] displays the deviation or modulation index of the current modulation function. For FSK or CPM modulations the meaning is straight forward. It identifies either the peak deviation or the modulation index of the modulation as indicated. For all other types of vector modulation, the power of the modulated waveform is defined by the constellation, the filtering, and the carrier power. However, in order to prevent clipping when waveforms are passed through the pulse shaping filters, the constellations are reduced by a factor of 7/16. The resulting scale is defined to have a scale factor of 1.0. Output power calibration assumes a scale factor of 1.0. Normally, this scale factor need not be changed, because the carrier power is set via the [AMPL] key. However, the user may alter this scale factor, if desired. Larger scale factors will use more of the available digital phase space and reduce the quantization noise of the final waveform. This might also be desirable if the amplitude is already at max power and you still need a bit more power. The risk is that the pulse shaping filters will occasionally clip the waveform to the rail during large excursions.

Pulse Shaping Filter

Pressing [SHIFT] [MOD DEV] enables one to select an appropriate pulse shaping filter for the modulation. Use the ADJUST [△] and [▽] keys to make the desired selection. The first three filter options, Nyquist, Root-Nyquist, and Gaussiain, actually represent a family of filters which can be customized with a bandwidth control factor. The bandwidth factor is usually denoted by α for Nyquist and Root-Nyquist filters, and by BT for Gaussian filters. The bandwidth control factor for these filters is modified via the "α or BT" secondary function, [SHIFT] [DC OFFS]. The bandwidth control parameters may vary from 0.1 to 1.0.

Modulation On/Off

Finally, the [ON/OFF] key toggles the modulation on and off. The current state is indicated by the ON/OFF LEDs.

Amplitude Shift Keying

Amplitude shift keying (ASK) is a modulation technique in which digital symbols are encoded in the amplitude of the RF. The phase is ignored. In the SG390 series generators ASK is implemented by only modulating the I channel and forcing the Q channel to zero.

Selecting ASK Modulation

Use the following steps to select ASK Modulation:

1. Press [MOD TYPE]
2. Press the ADJUST [△] and [▽] keys until the AM/ASK LED is highlighted.
3. Press the SELECT [◁] and [▷] keys until the VECTOR LED is highlighted with the desired modulation.

Simple Waveforms

As with analog modulation, the RF may be vector amplitude modulated with simple waveforms: sine, ramp, triangle, square, noise, and user waveforms. To select this type of modulation use the following steps:

1. Select ASK modulation using the steps outlined above.
2. Press the SELECT [◁] and [▷] keys until the display reads "Vector AM Func."

3. Press [MOD FCN]

4. Press the ADJUST [△] and [▽] keys to select the desired waveform.

Digital Constellations

The SG390 series generators provide four default constellations for use with 1-bit, 2-bit, 3-bit, and 4-bit digital modulation. Custom user constellations may also be downloaded if desired. The default constellations are summarized in Figure 49.

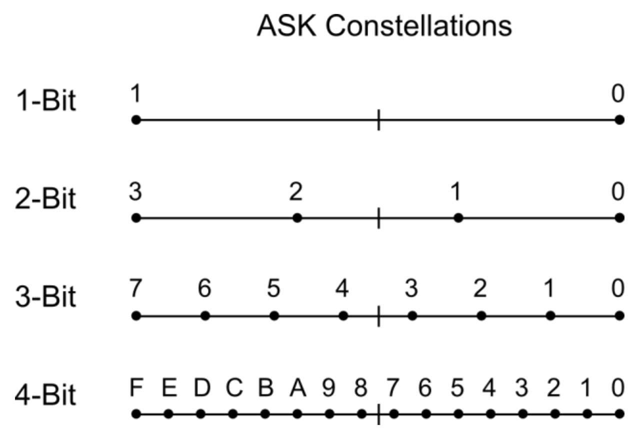


Figure 49: Default ASK symbol constellations.

To select a digital ASK modulation, follow the steps above for selecting ASK modulation and use the SELECT [◁] and [▷] keys to select the desired digital modulation. Waveforms for digital modulations include PRBS data, simple patterns and user data. Press [MOD FCN] and the ADJUST [△] and [▽] keys to select the desired waveform.

Frequency Shift Keying

Frequency shift keying (FSK) is a modulation technique in which digital symbols are encoded in the frequency of the RF. The amplitude of the carrier is held constant. In the SG390 series generators FSK is implemented using an internal rate generator followed by cosine/sine tables to convert a phase into its respective I and Q components.

Selecting FSK Modulation

Use the following steps to select FSK Modulation:

1. Press [MOD TYPE]

2. Press the ADJUST [△] and [▽] keys until the FM/FSK LED is highlighted.

3. Press the SELECT [◁] and [▷] keys until the VECTOR LED is highlighted with the desired modulation.

Simple Waveforms

As with analog modulation, the RF may be vector modulated in frequency with simple waveforms: sine, ramp, triangle, square, noise, and user waveforms. To select this type of modulation use the following steps:

1. Select FSK modulation using the steps outlined above.
2. Press the SELECT [◁] and [▷] keys until the display reads "Vector FM Func."
3. Press [MOD FCN]
4. Press the ADJUST [△] and [▽] keys to select the desired waveform.

Digital Constellations

The SG390 series generators provide four default constellations for use with 1-bit, 2-bit, 3-bit, and 4-bit digital modulation. Custom user constellations may also be downloaded if desired. The default constellations are summarized in Figure 50.

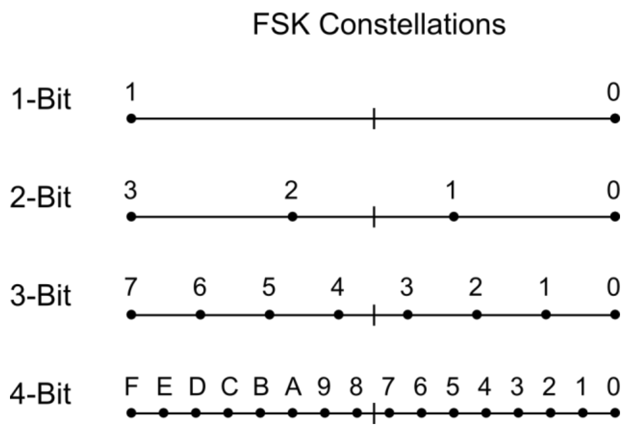


Figure 50: Default FSK symbol constellations.

To select a digital FSK modulation, follow the steps above for selecting FSK modulation and use the SELECT [◁] and [▷] keys to select the desired digital modulation. Waveforms for digital modulations include PRBS data, simple patterns and user data. Press [MOD FCN] and the ADJUST [△] and [▽] keys to select the desired waveform.

Frequency deviations of up to 6 MHz are supported. The configured deviation applies to symbol 0 in each of the constellations.

Phase Shift Keying

Phase shift keying (PSK) is a modulation technique in which digital symbols are encoded in the phase of the RF. The amplitude of each constellation point is the same. In spite of this, the modulation is not constant amplitude as it is for FSK. The pulse shaping filters create amplitude variations as the modulation traverses from symbol to symbol, creating waveforms very similar to QAM. In fact, vector PSK modulation may be considered a subset of QAM modulation.

Selecting PSK Modulation

Use the following steps to select PSK Modulation:

1. Press [MOD TYPE]

2. Press the ADJUST [△] and [▽] keys until the ΦM/PSK LED is highlighted.

3. Press the SELECT [◁] and [▷] keys until the VECTOR LED is highlighted with the desired modulation.

Simple Waveforms

The SG390 series generators support vector phase modulation with some simple waveforms. The supported waveforms are summarized in Table 26:

Table 26: Vector Phase Modulation Waveforms

Waveform	Description
Sin cos	Channel I is a sine wave and channel Q is a cosine wave. This combination moves the RF carrier down in frequency by the modulation rate.
Cos sin	Channel I is a cosine wave and channel Q is a sine wave. This combination moves the RF carrier up in frequency by the modulation rate.
Phase noise	Degrades the RF output with pure phase noise. The amplitude is held constant. The bandwidth and RMS deviation of the noise may be configured.
IQ noise	Degrades the RF output with IQ noise. The bandwidth of the noise may be configured. The noise power is equal to the RF carrier power when modulation is off.

To select this type of modulation use the following steps:

1. Select PSK modulation using the steps outlined above.

2. Press the SELECT [◁] and [▷] keys until the display reads “Vector PM Func.”

3. Press [MOD FCN]

4. Press the ADJUST [△] and [▽] keys to select the desired waveform.

Digital Constellations

The SG390 series generators provide four basic constellations and four specialized constellations. Custom user constellations may also be downloaded if desired. The constellations are summarized in Table 27.

Table 27: Phase Shift Key Constellations

Display	Standard Acronym	Bits/ Symbol	Comments
PM Binary	BPSK	1	Normal binary shift keying
PM Quadrature	QPSK	2	Normal quadrature shift keying
PM Quad Offset	OQPSK	2	Offset quadrature shift keying
PM Diff Quad	DQPSK	2	Differential quadrature shift keying
PM Pi4 Diff Quad	$\pi/4$ DQPSK	2	DQPSK with $\pi/4$ rotation
PM 3Pi8 3 bit	$3\pi/8$ 8 PSK	3	8 PSK with $3\pi/8$ rotation
PM 3 bit	8 PSK	3	Normal 8 PSK
PM 4 bit	16 PSK	4	Normal 16 PSK

To select a digital PSK modulation, follow the steps above for selecting PSK modulation and use the SELECT [◁] and [▷] keys to select the desired digital modulation. Waveforms for digital modulations include PRBS data, simple patterns and user data. Press [MOD FCN] and the ADJUST [△] and [▽] keys to select the desired waveform.

Basic PSK Constellations

The four basic PSK constellations are summarized in Figure 51. Be aware that the QPSK constellation follows a different mapping pattern than the 8 PSK and 16 PSK constellations. Since this constellation is identical to the QAM constellation of the same size, it uses the same mapping as well.

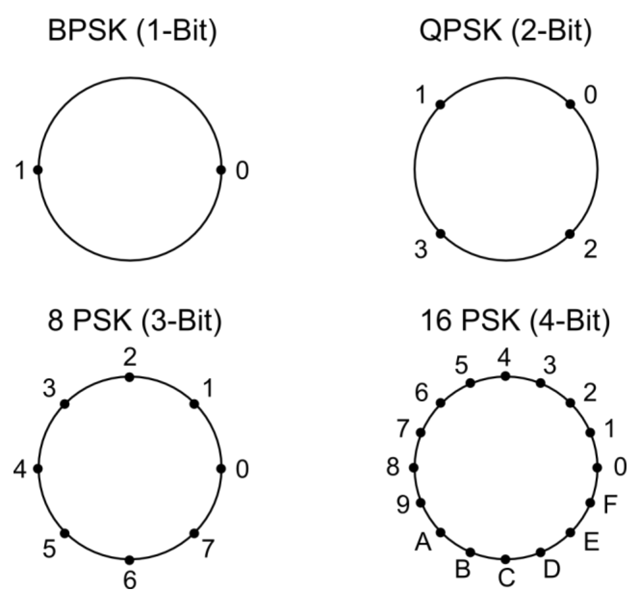


Figure 51: Basic PSK symbol constellations. Note that BPSK and QPSK follow the symbol mapping pattern used for QAM constellations.

Figure 52 shows an example demodulation of QPSK for an SG394 with the following setup:

Frequency:	1.00 GHz
Amplitude:	0.00 dBm
Waveform:	PRBS 7
Modulation:	QPSK
Rate:	100 kHz
Filter:	Root Nyquist, $\alpha = 0.3$

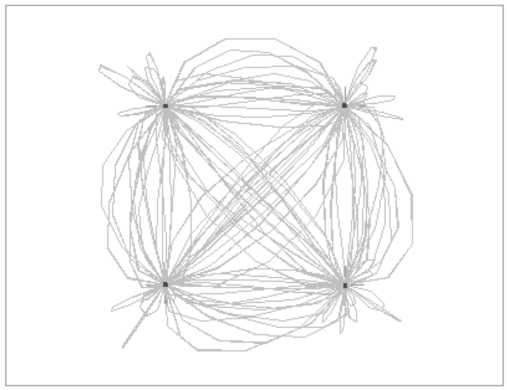


Figure 52: Agilent 89441A VSA demodulation of QPSK.

Note the small dark dots identifying the constellation points. A root-raised cosine filter combined with a root-raised cosine filter in the VSA produces a final demodulated waveform with virtually no intersymbol interference.

Specialized PSK Constellations

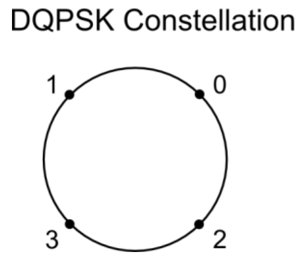
The SG390 series generators provide built-in support for four specialized PSK constellations listed in Table 27: OQPSK, DQPSK, π/4 DQPSK, and 3π/8 8 PSK. All of these constellations are variations of the basic PSK constellations intended to address specific problems in receiver design.

Differential Encoding of Symbols

One of the difficulties in receiving and decoding the basic PSK constellations is that the demodulation requires a coherent detector. The receiver must lock onto and track phase of the RF carrier for the entire transmission in order to successfully decode the transmitted message. Differential encoding of digital symbols enables the use of noncoherent receivers which are simpler and more cost effective to produce.

In differential encoding the information is encoded in the difference in phase from one symbol to the next, rather than in the phase itself. Receiver design is simplified because the receiver can use the phase of the last symbol as a reference for decoding the next symbol. It does not need to lock onto a stable reference over the entire transmission. Rather it only needs a reference that is stable from one symbol to the next, a much easier goal to meet. In fact, for DQPSK, the reference may simply be a delayed version of the signal itself.

The DQPSK constellation looks identical to the QPSK constellation but the interpretation is different. Data is differentially encoded, and so what matters is how the phase changes from one symbol to the next, not the current phase. Refer to Figure 53



Symbol	Encoding
0	No change in phase
1	+90° change in phase
2	−90° change in phase
3	180° change in phase

Figure 53: Decoding DQPSK transmissions.

Offset or Staggered Modulation

Offset modulation, also called staggered modulation, addresses a different problem in the communication design, this time with the transmitter. RF amplifiers can be made to operate much more efficiently if the signals they are amplifying are nearly constant in amplitude. This is especially important for satellites deployed in space. The difficulty is that the amplifiers have a nonlinear response in this regime. The nonlinearities are often not problematic as long as the amplitude variations are contained within a small band. Unfortunately, normal QPSK modulation does not meet this criterion. Remember that even though the constellation points are defined with constant amplitude, the RF amplitude varies as it transitions from one point to the next. For transitions of 180°, the signal power will momentarily go all the way down to zero. Nonlinear amplifiers forced to make such a transition will create out-of-band interference, thus, defeating the whole purpose of the pulse shaping filters.

Offset modulation addresses this problem by modifying the modulation to prevent a transition through the origin. See Figure 54.

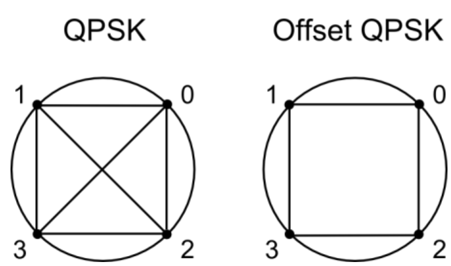


Figure 54: Offset modulation prevents transitions through the origin.

In normal QPSK modulation, I and Q data are shifted into the pulse shaping filters simultaneously. With offset or staggered modulation, the shifting of data for the two channels is offset by half a symbol period. First I is shifted in. One half a symbol period later, Q is shifted in. One half a symbol period later, the next I is shifted in, and so on. On the IQ plane, I transitions are strictly horizontal, and Q transitions are strictly vertical. However, since both transitions cannot happen simultaneously, the trajectory must follow the outside edges between constellation points. It can never go through the origin, thus, solving the problem.

Figure 55 shows an example demodulation of Offset QPSK for an SG394 with the following setup:

Frequency:	1.00 GHz
Amplitude:	0.00 dBm
Waveform:	PRBS 7
Modulation:	Offset QPSK
Rate:	100 kHz
Filter:	Root Nyquist, α = 0.3

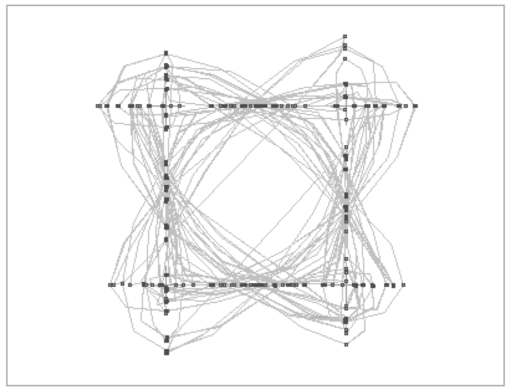


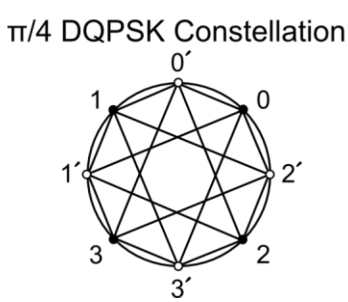
Figure 55: Agilent 89441A VSA demodulation of Offset QPSK.

First, note that the dark constellation points in the figure all line up on a rectangular grid. This is a consequence of the offset timing. When the I component of the RF is sampled, the Q component is half way through its next transition and completely undefined. The two allowed states for the I component are thus mapped into two horizontal lines. In a similar fashion, the two allowed states for the Q components are mapped into two vertical lines.

Second, note the lack of transitions passing through the origin. Compare this with the constellation presented in Figure 52 for QPSK. Offset timing is quite effective in preventing transitions through the origin, thus easing the linearity requirements of the transmitter.

Rotating Constellations

Offset modulation is not the only method of preventing transitions through the origin. The second commonly employed technique is to rotate the constellation after each symbol. This strategy is exemplified by the π/4 DQPSK and the 3π/8 8 PSK constellations.



Symbol	Encoding
0	+45° change in phase
1	+135° change in phase
2	−45° change in phase
3	−135° change in phase

Figure 56: π/4 DQPSK uses differential encoding and a rotating constellation.

Like DQPSK, π/4 DQPSK employs differential encoding, which means information is encoded in the change in phase, rather than the phase itself. However, the constellation for π/4 DQPSK rotates by 45° or π/4 radians after each symbol transmission. See Figure 56. Unprimed constellation points may only transition to primed constellation points and vice versa. The allowed transitions are indicated in the figure. Notice that none of the transitions pass through the origin, thus, solving the problem.

Figure 57 shows an example demodulation of π/4 DQPSK for an SG394 with the following setup:

Frequency:	1.00 GHz
Amplitude:	0.00 dBm
Waveform:	PRBS 7
Modulation:	π/4 DQPSK
Rate:	100 kHz
Filter:	Root Nyquist, α = 0.3

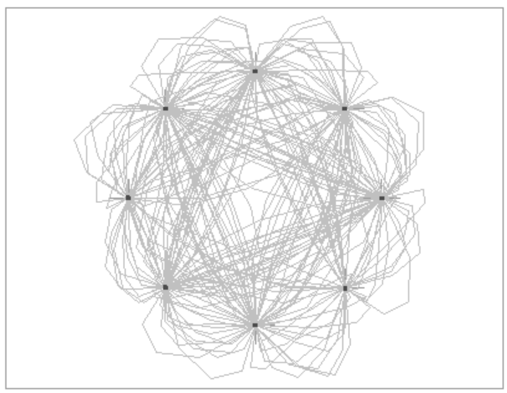


Figure 57: Agilent 89441A VSA demodulation of π/4 DQPSK.

First, note the small dark dots identifying the constellation points. There are a total of 8 constellation points, but only 4 of them are allowed at any given time due to rotation of the constellation after each symbol.

Second, note the low density of transitions passing through the origin. Although not as effective as offset timing, this modulation still compares favorably to the constellation presented in Figure 52 for QPSK. Rotating constellations is reasonably effective at preventing transitions through the origin.

The 3π/8 8 PSK constellation is similar in design to the π/4 DQPSK. In this case, data is not differentially encoded, but the constellation rotates to prevent transitions through the origin. In this case, the basic constellation is that of 8 PSK, except that the constellation rotates by 67.5° or 3π/8 radians after each symbol transmission. A version of this constellation with a Gray code mapping is used in the GSM EDGE mobile communication protocol. See Figure 58.

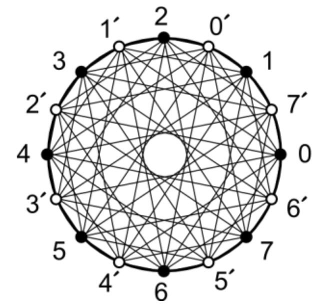


Figure 58: 3π/8 8 PSK follows standard 8 PSK, but the constellation rotates by 3π/8 after each symbol

Due to the rotation of the constellation, unprimed constellation points may only transition to primed constellation points and vice versa. The allowed transitions are indicated in the figure. Notice that none of the transitions pass through the origin, again solving the problem. The exclusion from the origin is smaller than for the π/4 DQPSK constellation, however. This constellation, therefore, places more stringent demands on the linearity of the transmitter.

Quadrature Amplitude Modulation

In quadrature amplitude modulation (QAM), both the amplitude and phase of the constellation points are varied, usually in a rectangular array. In all other respects, it is identical to phase shift keying.

Selecting QAM Modulation

Use the following steps to select QAM Modulation:

1. Press [MOD TYPE]
2. Press the ADJUST [△] and [▽] keys until the QAM LED is highlighted.
3. Press the SELECT [◁] and [▷] keys until the desired modulation is selected.

Waveforms for the modulation include PRBS data, simple patterns and user data. Press [MOD FCN] and the ADJUST [△] and [▽] keys to select the desired waveform.

QAM Constellations

The SG390 series generators provide default constellations for QAM 4, QAM 16, QAM 32, QAM 64, and QAM 256. The constellations are all arranged as rectangular arrays with a simple right to left and top to bottom naming pattern. See Figure 59. The front panel displayed power corresponds to the constellation points in the corners of the array. For QAM 32 it indicates the power of the "missing" point in each corner.

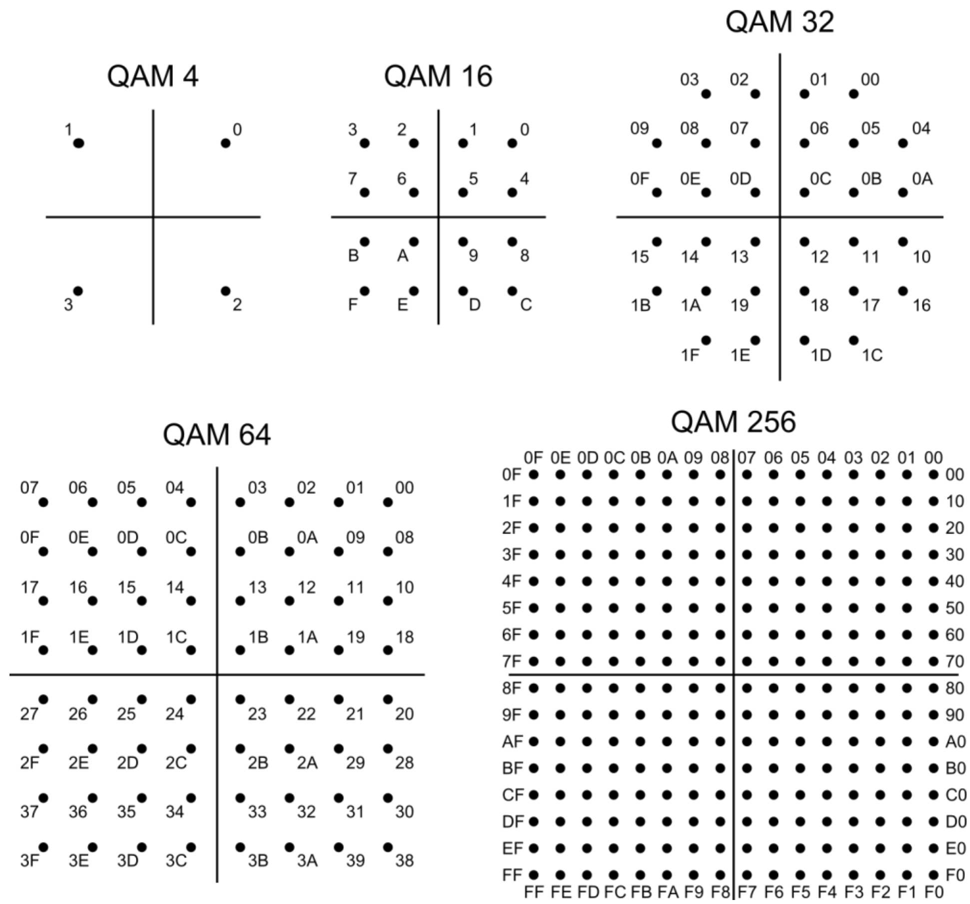


Figure 59: Constellations for QAM 4 through QAM 256.

Figure 60 shows an example demodulation of QAM 16 for an SG394 with the following setup:

Frequency:	1.00 GHz
Amplitude:	0.00 dBm
Waveform:	PRBS 7
Modulation:	QAM 16
Rate:	100 kHz
Filter:	Root Nyquist, α = 0.3

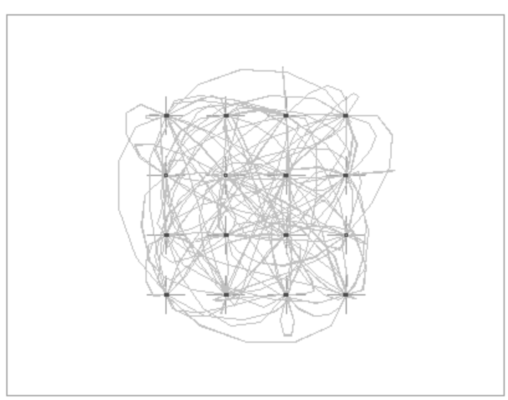


Figure 60: Agilent 89441A VSA demodulation of QAM 16.

Note the small dark dots identifying the 16 constellation points. A root-raised cosine filter combined with a root-raised cosine filter in the VSA produces a final demodulated waveform with virtually no intersymbol interference.

Continuous Phase Modulation

Continuous phase modulation (CPM) is a form of FSK modulation. Like FSK modulation, the RF carrier maintains a constant amplitude at all times. Only the phase is modulated. However, the general definition of FSK modulation allows for the phase to hop when the frequency is shifted. Such an allowance enables the creation of simple FSK modulators consisting of two independent oscillators and a multiplexer, driven by the data, switching between the two frequencies. When the multiplexer switches between the oscillators, both the frequency and the phase of the output change.

Continuous phase modulation, in contrast, guarantees that the phase will not suffer a discontinuous jump when switching to a new frequency. As the name implies, the phase will be continuous. The implementation of FSK in the SG390 series generators happens to be continuous phase, so in this respect, the two modulations are almost the same. Internally, however, the implementations have one distinct difference: the FSK implementation tracks frequency while the CPM implementation tracks phase. The FSK implementation allows arbitrary frequency deviations, but will, in general, slip phase relative to a fixed carrier. The CPM implementation, on the other hand, requires a rational modulation index, but will never slip phase. Aside from this, the two modulations are identical.

The following equation describes the correspondence between an FSK peak frequency deviation, F_{dev}, and a CPM modulation index, h:

$$h = \frac{2F_{dev}T}{2^N - 1}$$

where T is the symbol period and N denotes the number of bits per symbol.

Phase Trellis Diagram

As mentioned above, CPM modulation is a form of continuous phase FSK. However, it can also be viewed as a special form of offset phase shift keying, OPSK, with sinusoidal symbol weighting. Ultimately, this means that CPM transmissions may be decoded by demodulating the frequency or, alternatively, the phase. For binary CPM the phase will traverse $h\pi$ for every symbol transition. Thus, one can map out a trellis diagram of allowed transitions and phases over time. See Figure 61.

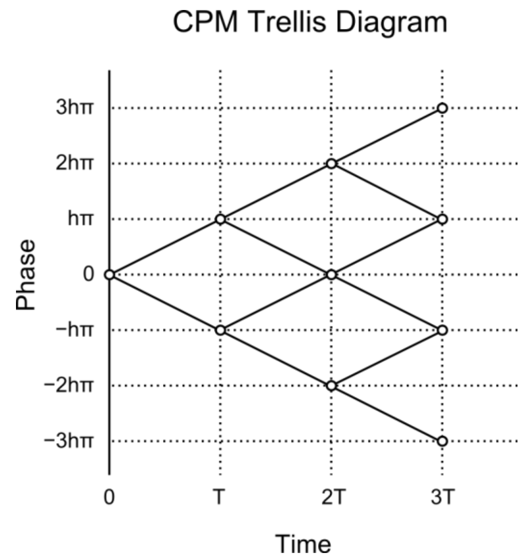


Figure 61: Phase trellis diagram for binary CPM with a rectangular filter.

Note that if h is a simple rational fraction, the allowed phases will map onto a finite number of allowed phases. For h = 1/2, for instance, there are only 4 allowed phases: 0, π/2, π, and 3π/2. Only 2 of the 4 phases are allowed at each transition, however.

MSK and GMSK Modulation

Minimum shift keying (MSK) and Gaussian minimum shift keying (GMSK) are perhaps the two most well known examples of CPM modulation. MSK is binary CPM with a modulation index, h = 1/2, and a rectangular filter. It derives its name from the fact that the two frequencies of the modulation have the minimum frequency separation allowed for orthogonal detection. The frequency separation is just ¼ of the symbol rate. Thus, it is one of the most bandwidth efficient types of modulation.

GMSK further improves the bandwidth efficiency of MSK, by replacing the rectangular filter with a Gaussian filter. GMSK with a bandwidth symbol time product of BT = 0.3 is used in the GSM mobile communications protocol.

Selecting CPM Modulation

Use the following steps to select CPM modulation:

1. Press [MOD TYPE]
2. Press the ADJUST [△] and [▽] keys until the CPM LED is highlighted.
3. Press the SELECT [◁] and [▷] keys until the desired modulation is selected.

Waveforms for the modulation include PRBS data, simple patterns and user data. Press [MOD FCN] and the ADJUST [△] and [▽] keys to select the desired waveform.

Modulation Index

Modulation indices for CPM modulation may be specified to 3 decimal digits, but internally the value is rounded to the nearest rational factor, n/512, where n is an integer.

Thus, if one wishes to obtain a modulation index of 7/16 = 0.4375, one should enter 0.438. Internally, the instrument will round the result to 224/512 = 7/16.

CPM Constellations

The SG390 series generators provide four default constellations for use with 1-bit, 2-bit, 3-bit, and 4-bit digital modulation. Unlike the other modulation modes, these constellations are fixed and cannot be changed. The constellations are summarized in Figure 62.

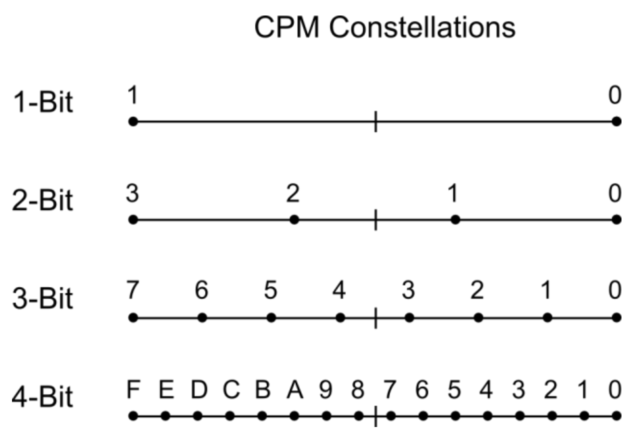


Figure 62: Default CPM symbol constellations.

Figure 63 shows an example demodulation of GSM for an SG394 with the following setup:

Frequency:	1.00 GHz
Amplitude:	0.00 dBm
Waveform:	PRBS 7
Modulation:	CPM 1-bit
Rate:	270.833 kHz
Filter:	Gaussian, BT = 0.3

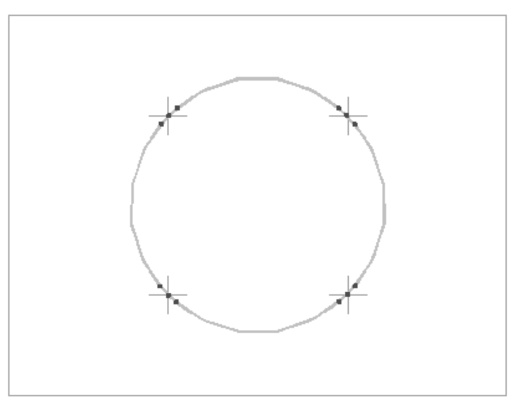


Figure 63: Agilent 89441A VSA demodulation of GSM.

GSM uses Gaussian minimum shift keying (GMSK), which is a Gaussian filtered version of MSK. This is a binary CPM modulation with h = 1/2. Although there are only 2 allowed states at each transition, there are a total of 4 allowed phases in the phase tree. Notice that each constellation point in the figure is actually made up of a set of 3 points.

This is due to the fact that Gaussian filters do not eliminate intersymbol interference (ISI). The extra 2 dots are due to the interference of the nearest neighboring symbols. Also notice that the transitions between symbols fall on a circle, showing that the modulation is of constant amplitude.

Vestigial Sideband Modulation

Vestigial sideband modulation (VSB) is a form of amplitude modulation used in the over-the-air transmission of digital television (DTV) in the United States. Amplitude modulation normally creates two sidebands: an upper sideband and a lower sideband. However, the information content in the upper sideband is identical to that of the lower sideband. Thus, one can increase the bandwidth efficiency of the modulation by nearly a factor of two, without loss of information by filtering out the lower sideband. This is referred to as single sideband amplitude modulation (SSB AM). In practice, however, it is very difficult to completely filter out the lower sideband. A vestigial portion of the lower sideband is often still present, hence the name vestigial sideband modulation.

Receivers required to demodulate VSB need to lock onto a clean reference frequency. To facilitate this, the ATSC digital television standard stipulates the addition of a pilot tone to the modulation at the carrier frequency. The pilot tone is located at the lower edge of the VSB spectrum. The standard describes 2 versions of the modulation to be used for over-the-air transmissions: 8 VSB, and 16 VSB. Both modulation types are supported by the SG390 series generators at modulation rates of up to 12 MHz. The transmission rate required by the DTV standard is $4.5 \times 684 / 286 \cong 10.762$ MHz.

Selecting VSB Modulation

Use the following steps to select VSB modulation:

1. Press [MOD TYPE]

2. Press the ADJUST [△] and [▽] keys until the VSB LED is highlighted.

3. Press the SELECT [◁] and [▷] keys until the desired modulation is selected.

Waveforms for the modulation include PRBS data, simple patterns and user data. Press [MOD FCN] and the ADJUST [△] and [▽] keys to select the desired waveform.

VSB Constellations

The SG390 series generators provide two constellations for use with 8 VSB and 16 VSB modulation.. Unlike the other modulation modes, these constellations are fixed and cannot be changed. The constellations are summarized in Figure 64.

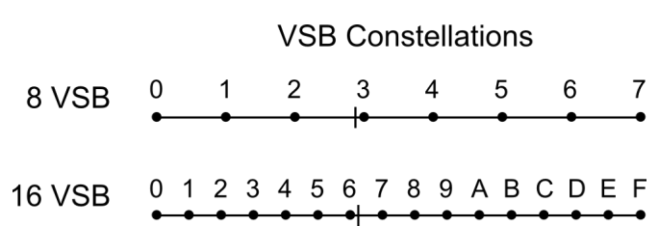


Figure 64: VSB symbol constellations.

Notice that the constellations are not symmetric about the origin. They have been shifted to the right. This bias in the constellation is what creates the pilot tone required by the standard.

Figure 65 shows an example demodulation of 8 VSB for an SG394 with the following setup:

Frequency:	1.00 GHz
Amplitude:	0.00 dBm
Waveform:	PRBS 9
Modulation:	8 VSB
Rate:	10.762 MHz
Filter:	Root-Nyquist, α = 0.115

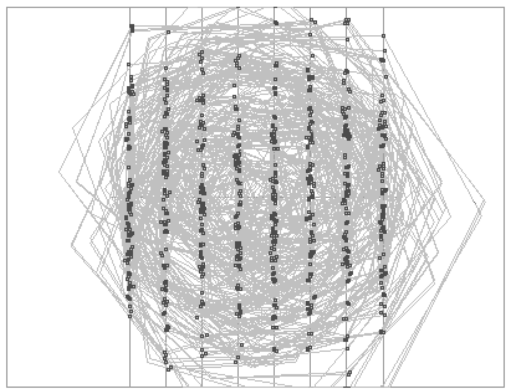


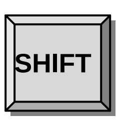
Figure 65: Agilent 89441A VSA demodulation of 8 VSB.

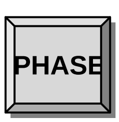
As mentioned above, 8 VSB modulation is a form of amplitude modulation. There are only 8 allowed states for the I component of the RF. However, due to the filtering of the lower sideband, the Q component is completely undefined. Thus, the constellation on the IQ plane is represented by 8 vertical lines.

Additive White Gaussian Noise

All digital modulations may be optionally degraded by additive white Gaussian noise (AWGN). The noise is inserted just before the pulse shaping filters. See Figure 47. The noise may range in power from –10 dB to –70 dB relative to the maximum power of a constellation.

Selecting AWGN





AWGN is configured via the secondary function “Add. Noise.” Press the keys [SHIFT] [PHASE] and then use the ADJUST [△] and [▽] keys to toggle the noise power on and off. Press SELECT [▷] to view and adjust the noise power. Enter the desired noise power via the numeric key pad. Noise powers from -10 dB to -70 dB may be entered. This gives one the ability to create typical error vector magnitudes (EVM) ranging from 32 % to 0.32 %, respectively.

Figure 66 shows an example demodulation of QAM 16 constellation which has been degraded by AWGN. The SG394 had the following setup:

Frequency:	1.00 GHz
Amplitude:	0.00 dBm
Waveform:	PRBS 7
Modulation:	QAM 16
Rate:	100 kHz
Filter:	Root Nyquist, α = 0.3
AWGN	–25 dB

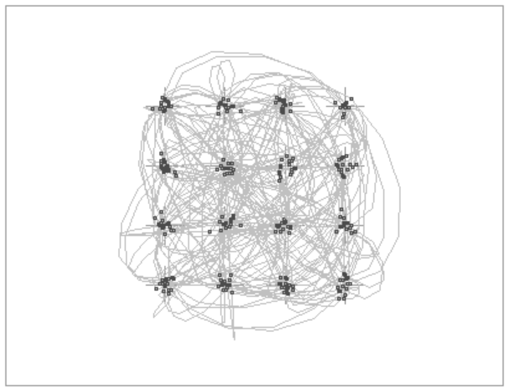


Figure 66: Agilent 89441A VSA demodulation of QAM 16 with –25 dB of AWGN.

–25 dB of AWGN is enough noise to create an error vector magnitude (EVM) of about 5.6 %. Compare the sharp constellation points of Figure 60 to those of Figure 66. The noise degradation is quite visible in the figure.

External IQ Modulation

The SG390 series generators may be modulated via an external source with bandwidths above 100 MHz if desired. Rear panel BNC inputs are available as I and Q signal inputs. The inputs are terminated into 50 Ω with full-scale amplitude of 0.5 V.

Selecting External IQ Modulation

Use the following steps to select external IQ Modulation:

1. Press [MOD TYPE]
2. Press the ADJUST [△] and [▽] keys until the QAM LED is highlighted.
3. Press [MOD FCN]
4. Press the ADJUST [△] and [▽] keys until the front panel display reads “Fn Rear IQ Input” and the EXT LED is highlighted.

Note that an external vector modulation option is available for ASK, PSK, and QAM modulation modes. The options are identical in all modes and are available merely as a convenience to the user.

Arbitrary Waveform Generation

Introduction

The SG390 series generators provide a broad array of built-in support for the most common digital modulation formats, constellations, and filters. However, the user may choose to download custom waveforms, constellations, and filters over the remote interface if the built-in support does not match his needs. This chapter describes the file formats expected by the instrument when downloading user generated data. Details about how to communicate with the instrument over a remote interface are given in the Remote Programming chapter starting on page 87.

Downloading Binary Data

User waveforms, constellations, and filters can contain a considerable amount of data. In order to improve the efficiency of transfer, the data is sent in binary format. The remote commands that accept binary data follow the syntax for an IEEE 488.2 definite length <ARBITRARY BLOCK PROGRAM DATA>. This message element has the following format:

<arb data> = #[ASCII digit 1 to 9][ASCII digit 0 to 9]+[Binary Data]

The message element has 4 parts to it:

1. The ASCII character '#'.
2. An ASCII digit from '1' to '9'. This digit identifies the number, M, of ASCII digits that follow.
3. M bytes containing ASCII digits from '0' to '9' that identify the number, N, of binary bytes that follow.
4. N bytes of binary data.

An example should make this clear. The following block transmits the 26 ASCII bytes from 'A' to 'Z':

#3026ABCDEFGHIJKLMNOPQRSTUVWXYZ

The first two characters indicate that an arbitrary block of data follows and that the length of the block is given by the following 3 digits, '026'. These digits indicate that the binary message is 26 bytes long. The actual data follows. For clarity, only printable characters were used in this example, but arbitrary 8-bit binary data may be transmitted as part of an <arb data> block.

Big-Endian Byte Order

In many cases, 16-bit or 32-bit numbers must be encoded in a binary transmission. The native encoding for numbers in computers follows one of two common formats: little-endian and big-endian. The SG390 series generators expect data in a big-endian format. Most Intel based computers natively store numbers in a little-endian format. For these machines, all binary numbers will have to be converted into a big-endian format before being transmitted.

As an example, the decimal number 43,891 is represented by the hexadecimal value 0xABCD. Storage of this number within the memory of a computer, however, depends on the native storage format: In the big-endian format the number is stored as the bytes AB CD. In the little-endian format, however, the number is stored as the bytes CD AB, i.e. the bytes are swapped. Numbers stored in this format will need to be swapped back into big-endian format before being transmitted over the remote interface.

SRAM vs Flash Storage

The SG390 series generators include 2 MB of SRAM and Flash for storage of arbitrary waveforms, constellations, and filters. SRAM is volatile memory that is lost when power is removed from the instrument. Flash is nonvolatile memory that is retained even when power is cycled. User data is always downloaded into SRAM first. Once downloaded, the user may optionally copy the data into flash if desired with one of the commands SAVW, SAVC, or SAVF. Waveforms may be played directly out of SRAM or flash.

Arbitrary User Waveforms

The SG390 supports two different formats for arbitrary user waveforms: as a stream of digital bits, or as a series of 16-bit I/Q values. The former is much more efficient than the latter and is the preferred choice, if possible. In both cases, data is transmitted in 16-bit chunks with the following command:

WRTW i, j, <arb data>

Parameter i is a 32-bit value indicating the configuration format of the user data. The configuration bits are described in Table 28.

Table 28: Arbitrary waveform configuration word

Bit	**31-9**	**8**	**7-6**	**5-0**
Meaning	reserved	analog	reserved	bits/symbol

Bits/symbol may be one of the values 1 to 9, 16, or 32. Use 32 for vector waveforms consisting of 16-bit, IQ value pairs that bypasses the symbol reader and constellation mapping. Use 16 for analog and vector waveforms that bypass the symbol reader and constellation mapping. Bit 8 should be set if the waveform is intended for analog modulation. All other bits should be cleared.

Parameter j is a 32-bit value indicating the total number of bits in the waveform.

<arb data> contains the binary data representing the data and it must contain an even integer number of bytes. Waveforms have a minimum size of 16 bits and are played

back from MSB to LSB. If a waveform does not end on a 16-bit boundary, the least significant bits of the last word in the waveform will be ignored. The following example should clarify the issues:

WRTW 4, 28, #14XXXX

The first parameter indicates that the waveform consists of 4-bit symbols for vector modulation. The second parameter indicates that there are 28 bits in the total waveform. The third parameter indicates that 4 bytes, or 32-bits, of binary data are transmitted. Since the full waveform consists of 28 bits, the 4 least significant bits of the last 16-bits of transmitted data will be ignored. 4 bytes are transmitted because this is the minimum even integer of bytes which fully contains the waveform.

Packing Symbols into a Waveform

As mentioned above, when a waveform is played back, symbols are read out of memory from the most significant bit to the least significant bit. Suppose we wanted to transmit the following ten, 2-bit symbols:

2,0,2,1,3,1,0,2,1,3

When translated to binary, these symbols become the following:

10, 00, 10, 01, 11, 01, 00, 10, 01, 11

The symbols need to be packed into 8-bit bytes. This is accomplished by concatenating the binary symbols together into an even number of bytes:

10001001, 11010010, 01110000, 00000000

The last 2 symbols did not contain enough data to produce a complete byte. Therefore, binary zeros were added to complete the byte. An additional byte of binary zeros was added to ensure the waveform was packed into an even number of bytes. In hexadecimal format, the waveform contains the following bytes:

89 D2 70 00

Having this, the final waveform download command can be synthesized as the following:

WRTW 2, 20, #14<89 D2 70 00> <NL>

The first parameter indicates we have 2 bit symbols. The second parameter indicates that the full waveform is 20 bits long. The last parameter indicates we are transmitting 4 bytes of data. The portion inside the brackets indicates the 4 bytes transmitted. The brackets are not part of the transmission. Finally, all commands must be terminated with a semicolon, a carriage return <CR>, or a new-line <NL>. This command is no exception. Thus, a <NL>, which has the hexadecimal value 0x0A, follows the 4 binary bytes.

Packing 16-bit IQ Data into a Waveform

Instead of playing back pure digital data, the SG390 series generators can optionally accept raw IQ values, and bypass the symbol reader and constellation mapping functions. This mode is active when the modulation subtype is set to ‘vector function’ rather than identifying a specific constellation: 1-bit, 2-bit, etc.

The instruments accept 16-bit, 2’s complement binary data for I and Q. Values may range from –32768 to +32767. If both I and Q are being specified, then for each point, I is specified first, followed by Q.

Suppose we wanted to transmit the following 4, IQ data pairs:

(32767, 16384), (8192, –8192), (–16384, 4096), (–32768, –4096)

In hexadecimal format the data pairs have the following values:

(0x7FFF, 0x4000), (0x2000, 0xE000), (0xC000, 0x1000), (0x8000, 0xF000)

The data pairs are packed into a binary stream of bytes with the 16-bit value for I presented first followed by the 16-bit value for Q. The 16-bit values must be packed in the big-endian format. We have 4, IQ data pairs, with 16 bits of data each, giving a total waveform of 4 × 2 × 2 = 16 bytes. The hexadecimal bytes for the waveform follow:

7F FF 40 00 20 00 E0 00 C0 00 10 00 80 00 F0 00

Having this, the final waveform download command can be synthesized as the following:

WRTW 32, 128, #216<7F FF 40 00 20 00 E0 00 C0 00 10 00 80 00 F0 00> <NL>

The first parameter indicates we have 32-bit symbols: 16 bits for I and 16 bits for Q. The second parameter indicates the total waveform is 128 bits long. The last parameter indicates we are transmitting 16 bytes of data. The portion inside the brackets indicates the 16 bytes transmitted. The brackets are not part of the transmission. Finally, all commands must be terminated with a semicolon, a carriage return <CR>, or a new-line <NL>. This command is no exception. Thus, a <NL>, which has the hexadecimal value 0x0A, follows the 16 binary bytes.

Saving Waveforms to Nonvolatile Memory

Once a waveform has been downloaded to internal SRAM, it may be saved into nonvolatile memory. Space permitting, up to 9 waveforms may be stored in nonvolatile memory. All waveforms have an event marker file associated with them. Waveforms are stored in nonvolatile memory together with their associated event marker file. Once stored in nonvolatile memory, a waveform must be deleted before the memory occupied by the waveform is available for new waveforms.

A waveform downloaded into SRAM may be saved into nonvolatile memory with the following command:

SAVW? i

The parameter i identifies the location for the saved waveform. It should be an integer in the range from 1 to 9. Upon completion, the command returns an error code followed by the current available space in nonvolatile memory in 16-bit words. If successful, the error code will be 0. The most common errors include:

Table 29: Save waveform errors

Error Code	Name	Description
0	SUCCESS	Waveform saved successfully
80	FSERR_NO_MEMORY	Not enough space to save waveform
81	FSERR_NO_FILE	No source waveform in SRAM

Refer to the section Error Codes on page 126 for a complete listing of error codes.

Deleting Waveforms

A waveform stored in nonvolatile memory may be deleted with the following command:

DELW? i

The parameter i indicates the location of the waveform to delete. It may range from 0 to 9. Location 0 refers to any waveform stored in SRAM. Locations 1 to 9 identify waveforms stored in nonvolatile memory. Upon completion, the command returns an error code followed by the current available space in nonvolatile memory in 16-bit words. If successful, the error code will be 0. This command succeeds even if no waveform exists at the given location.

All waveforms stored in nonvolatile memory may be deleted with the following command:

ERAS?

This command frees all available memory for waveform storage. Upon completion, the command returns an error code followed by the current available space in nonvolatile memory in 16-bit words. If successful, the error code will be 0.

Listing Waveforms

A catalog listing of all available waveforms may be retrieved with the following command:

CATL?

The returned listing consists of a comma separated list of location followed by waveform size in 16-bit words. Location 0 refers to any waveform downloaded to SRAM. Locations 1 to 9 refer to user saved waveforms. Locations 10 and above refer to read-only waveforms preloaded at the factory. When all waveforms and sizes have been listed, the total available space for user waveform storage in 16-bit words is appended.

User Constellations

The SG390 series generators have the ability to process pure digital data by dynamically mapping digital symbols into IQ constellation points in real time. The symbol mapping is quite versatile and can easily accommodate differential encoding and rotating coordinate systems. The mapping is performed with the data from two tables stored in RAM: a symbol table, and a symbol set table. The basic architecture is diagrammed in Figure 67.

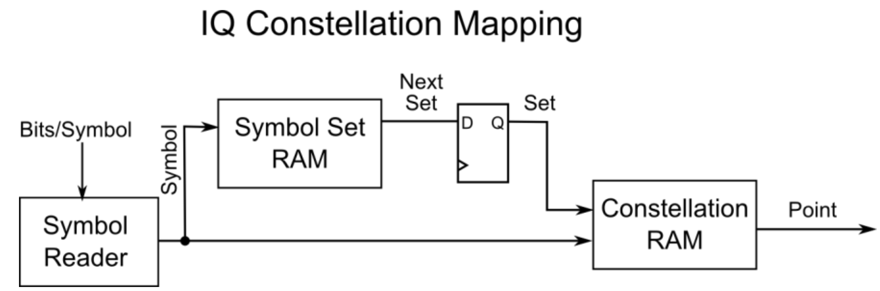


Figure 67: Architecture for mapping digital symbols into IQ constellation points.

The constellation RAM is 1kW in size which provides space to define up to 512, 32-bit, IQ constellation points with each point allocating 16 bits for I and 16 bits for Q. Associated with each symbol is a symbol set. Thus, the constellation RAM is accompanied by 512 bytes of symbol set RAM which defines the symbol set to associate with the following symbol.

The constellation RAM is accessed with a 9-bit address that is the concatenation of a (9 – N)-bit symbol set and an N-bit symbol. The address is computed from the current symbol and set via the equation

constellation address = (symbol + set × 2^N) mod 512

where N is the number of bits per symbol. As an example, suppose the symbol reader is reading in 2-bit symbols and that the current symbol is 3 and that the current symbol set is 5. The symbol will be mapped to the constellation point stored at address $3 + 5 \times 2^2 = 23$. At startup the first symbol set is initialized to zero.

For simple constellations, symbol set RAM is cleared and the symbol maps directly to a constellation point. For a constellation that rotates by π/4 after each symbol, we will have 8 different constellations before the constellation has rotated by exactly 2π. For N-bit symbols, the rotation is accomplished by filling symbol set RAM with 2^N 1s, followed by 2^N 2s, followed by 2^N 3s, etc until we reach 2^N 7s, followed by 2^N 0s. For differential encoding, the encoding of the next symbol is determined by the previous symbol. In this case, each symbol gets mapped to a different constellation, and so we have 2^N different constellations.

For each user constellation, two parameters must be declared: bits/symbol and whether the I and Q points in the constellation are to be staggered or not. Most constellations do not operate in staggered mode; both I and Q points enter their respective pulse shaping filters simultaneously. Staggered mode is required for offset modulation in which the Q values shift into their filter half a symbol after the I values have shifted.

User constellations are downloaded into SRAM with the following command:

WRTC i, j, <arb data>

Parameter i indicates the number of bits/symbol, N. It will normally range from 1 to 9. A value of 16 or 32 is accepted to enable staggered modulation when constellation mapping is bypassed. Parameter j indicates whether staggered operation is desired. Set j = 1 for staggered operation, otherwise set j = 0. <arb data> should be a definite arbitrary block with 2560 bytes of binary data. The <arb data> block is organized as 512 32-bit IQ pairs followed by 512 bytes of symbol set data. Each 32-bit IQ pair consists of a 16-bit I value followed by a 16-bit Q value in a big-endian format.

Example Constellation

As an example let us compute the constellation for QPSK with the symbol mapping defined in Figure 68.

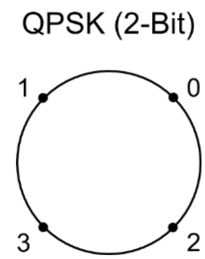


Figure 68: Default QPSK constellation.

The points lie on a circle of constant amplitude. The radius of the circle is 32767. Thus, we can compute the IQ coordinates as shown in Table 30.

Table 30: QPSK constellation point computations

Symbol	Formula	Value	Hex Values
0	32767 (cos(π/4), sin(π/4))	(23170, 23170)	(5A82, 5A82)
1	32767 (cos(3π/4), sin(3π/4))	(–23170,23170)	(A57E, 5A82)
2	32767 (cos(7π/4), sin(7π/4))	(23170,–23170)	(5A82, A57E)
3	32767 (cos(5π/4), sin(5π/4))	(–23170,–23170)	(A57E, A57E)

Note that we need only define 4 constellation points. All others may be set to zero, since they will not occur for 2-bit waveforms. Furthermore, since the constellation does not change from symbol to symbol, we should zero out all symbol set RAM as well.

Combining all this information together we can synthesize the following command to download the constellation:

WRTC 2, 0, #42560<5A 82 5A 82 A5 7E 5A 82 5A 82 A5 7E A5 7E A5 7E…><NL>

The first parameter indicates this is a 2-bit constellation. The second parameter indicates that the IQ values are not staggered. The third parameter indicates that we are transmitting 2560 binary bytes. The portion inside the brackets shows the first 16 bytes of the transmission. These bytes represent our 4 constellation points. The following 2544 bytes are all zero. The brackets are not part of the transmission. Finally, all commands must be terminated with a semicolon, a carriage return <CR>, or a new-line <NL>. This command is no exception. Thus, a <NL>, which has the hexadecimal value 0x0A, follows the 2560 binary bytes.

Saving Constellations to Nonvolatile Memory

Once a constellation has been downloaded to internal SRAM, it may be saved into nonvolatile memory, if desired. A constellation is saved into nonvolatile memory with the following command:

SAVC? i

The parameter i refers to the location into which the constellation is stored. It may range from 1 to 9. Upon completion, the command returns an error code. If successful, the error code will be 0.

Note that this command will overwrite any previous constellation stored in that location.

User Filters

The SG390 series provides built-in support for several commonly used digital filters. The user also has the option to download custom filters, if desired. The filters have 24 symbols of memory and are defined with an oversampling ratio of 128, which means they are composed of 24 × 128 = 3072 coefficients. The large oversampling ratio is a consequence of the fact that the filters also play an integral part in the re-sampling of waveforms being played back at an arbitrary rate. Large oversampling ratios enable accurate re-sampling with simple, linear interpolation in a Farrow filter structure.

Internally, filter coefficients are stored with 17 bits of precision, but transmitted with 16 bits of precision along with a global 16-bit offset. This helps facilitate the binary transfer without compromising overall precision. Coefficients should be scaled so that the 17-bit value +32768 is equivalent to 1.000.

User filters are downloaded to SRAM using the following command:

WRTF i, <arb data>

Parameter i defines a 16-bit global offset. This 16-bit value is added to each 16-bit coefficient transmitted in <arb data> to produce the final 17-bit filter coefficient stored in the instrument. <arb data> should be a definite arbitrary block with 6144 bytes of binary data. The <arb data> block contains the 3072, 16-bit filter coefficients for the filter. Each of these coefficients is combined with the 16-bit global offset to produce 3072, 17-bit filter coefficients which are stored in the instrument.

Most filters are symmetric and peak at the center, but these are not requirements. However, the event markers and TDMA control engine within the FPGA assume a 12 symbol latency for the filter. Filters shorter than 24 symbols are easily accommodated by padding the filter with zeros at the beginning and the end.

Creating User Filters

As an example, we can create a windowed sinc filter using the following pseudo code:

```
# Number of coefficients
N = 3072
# Over sampling ratio
OSR = 128
# Kaiser filter parameter
ALPHA = 2.5
BETA = PI * ALPHA
# Create floating point array filled with integers from 0 to 3071
s = arange( float(N) )
# Rescale and offset array to cover range from -12.0 to +12.0
s = (s - N/2)/OSR
# Replace with the normalized sinc function
s = sinc( s )
# Get desired Kaiser window
```

```
w = get_window( ("kaiser",BETA), N )
# Window the sinc to create the filter
filter = s * w
# Scale filter to 32768 and truncate
filter = round( 32768 * filter )
# Create 16 bit offset
offset = 16384
# Subtract offset so that all coefficients are 16 bits
filter = filter - offset
```

In the above code, the sinc() function is the normalized version defined by

$$sinc(x) = \frac{\sin(\pi x)}{\pi x}$$

It is 1.0 at x = 0 and zero at all nonzero, integer values of x. The window is a Kaiser window with $\beta = \pi\alpha$ and $\alpha = 2.5$.

The very last statement in the code subtracts an offset from all the coefficients. This offset is only necessary to ensure that all coefficients are 16 bits during the binary transmission to the instrument. This offset will be added back to the coefficients by the instrument during the filter download. Thus, the coefficients values stored in the instrument equal the coefficients stored in filter before the offset is subtracted.

After the last statement of code, the filter variable should contain an array of 3072, 16-bit coefficients. The coefficients should be written into the <arb data> block in the big-endian format for transmission to the instrument.

Thus, we can synthesize the following command to download the filter to the instrument:

WRTF 16384, #46144<filter coefficients in big-endian format><NL>

The first parameter indicates the offset that should be added to each coefficient before storage into the instrument. The second parameter indicates that we are transmitting 6144 bytes of binary data. The portion inside the brackets represents the 6144 bytes of binary filter coefficient data. The brackets are not part of the transmission. Finally, all commands must be terminated with a semicolon, a carriage return <CR>, or a new-line <NL>. This command is no exception. Thus, a <NL>, which has the hexadecimal value 0x0A, follows the 6144 binary bytes.

Saving Filters to Nonvolatile Memory

Once a filter has been downloaded to internal SRAM, it may be saved into nonvolatile memory, if desired. A filter is saved into nonvolatile memory with the following command:

SAVF? i

The parameter i refers to the location into which the filter is stored. It may range from 1 to 9. Upon completion, the command returns an error code. If successful, the error code will be 0.

Note that this command will overwrite any previous filter stored in that location.

Event Markers and TDMA

Event markers provide a means for synchronizing external equipment with a modulation waveform. A symbol clock and three event marker signals are available on the back panel of the instrument. The symbol clock output produces a square wave clock signal at the symbol rate. The rising edge of the clock aligns with the peak response of the symbol in the pulse shaping filter. At each rising edge of the symbol clock, the event markers may be programmed to pulse high or low.

Event markers are programmed via a sequence of up to 512, 32-bit configuration words. Each word has the following meaning:

Table 31: Event marker configuration word

Bit	**31**	**30**	**29-0**
Meaning	Repeat	Action	Offset

Bits 29 to 0 define a symbol offset. During initialization, a symbol counter is initialized to zero. At each rising edge of the symbol clock, the symbol counter is incremented. When the symbol count equals the offset given in the configuration word, the action in bit 30 is performed. If Action = 1, the event marker is forced high, otherwise it is forced low. If the symbol count does not equal the offset, no action is taken and the state of the marker is left unchanged. After each successful symbol count comparison, the next configuration word is loaded, until the repeat bit is set, at which point the symbol counter is reset and the first configuration word reloaded. Each event marker has space for 512 event configuration words. For proper initialization, however, the first configuration word must have Offset = 0.

This simple system provides the flexibility to program markers that pulse high and low on every other symbol, or just once every million symbols. The symbol counters for each marker are independent, so we can have marker 1 pulsing high and low on every other symbol, but marker 2 independently pulsing high and low on every 10^{th} symbol.

TDMA

The SG390 series generators support Time Domain Multiple Access (TDMA) waveforms by associating an event marker with the RF power of output. When the marker is high, RF power is slowly ramped up to full power. When the marker is low, RF power is slowly ramped down and turned off. In the transition region the amplitude of the RF follows a raised cosine profile with a configurable period of 1, 2, 4, or 8 symbols. Once initiated, a ramp must complete before it may reversed, regardless of what the event marker it is associated with requests.

TDMA support is configured when the event marker files are downloaded via its own configuration word defined in Table 32:

Table 32: TDMA configuration word

Bit	**31-18**	**17-16**	**15-12**	**11-8**	**7-1**	**0**
Meaning	reserved	Mux	reserved	Ramp	reserved	Enable

Set bit 0 to enable TDMA functionality. Set Ramp to 1, 2, 4, or 8 for RF power ramp profiles that last the given number of symbol periods. Finally, set Mux to 1, 2, or 3 to associate the given marker with TDMA functionality. For simplicity the entire configuration word may be set to zero if TDMA is not used.

Default Marker Configuration

Marker configurations are always associated with a user waveform. When a user waveform is downloaded, a default marker configuration is automatically created for it. The newly created configuration replaces any other configuration that may have been active. The default marker configuration for a user waveform pulses Marker 1 high for one symbol period at the start of the waveform. Markers 2 and 3 are configured to stay low. TDMA is turned off. This default marker configuration is also used for PRBS and pattern waveforms, but in that case the configuration is fixed and cannot be modified.

Downloading Event Marker Configurations

Event marker configurations are downloaded with the following command:

WRTE i, <arb data>

Parameter i indicates the desired TDMA configuration word defined in Table 32. <arb data> should be a definite arbitrary block with 6144 bytes of binary data. The binary data consists of three sequences of 512 event configuration words. The first sequence is for Marker 1, the next sequence is for Marker 2, and the last sequence is for Marker 3. The individual event configuration words are defined in Table 31. Each 32-bit configuration word must be formatted as big-endian for the transmission.

Example Event Marker Configuration

Suppose we wish to create a marker configuration that pulses Marker 1 high for 1 symbol period at the beginning of a waveform and that our waveform is 1500 symbols long. We create our event configuration words for Marker 1 as shown in Table 33

Table 33: Example marker configuration sequence

Word	Repeat	Action	Offset	Configuration
0	0	1	0	0x40000000
1	0	0	1	0x00000001
2	1	0	1499	0x800005DB
3 to 511	0	0	0	0x00000000

Markers 2 and 3 consist of all zeros. We may now synthesize the event marker configuration command as follows:

WRTE 0, #46144<40 00 00 00 00 00 00 01 80 00 05 DB 00 00 00 00…><NL>

The first parameter indicates that TDMA is not used. The last parameter indicates we are transmitting 6144 bytes of binary data. The portion inside the brackets indicates the first 16 bytes of the transmission. The subsequent 6128 bytes are all zero. The brackets are not part of the transmission. Finally, all commands must be terminated with a semicolon, a carriage return <CR>, or a new-line <NL>. This command is no exception. Thus, a <NL>, which has the hexadecimal value 0x0A, follows the 6144 binary bytes.

Saving Event Markers to Nonvolatile Memory

Event markers are always associated with a waveform. Thus, when a user waveform is saved to nonvolatile memory, the event marker associated with it is also saved. No extra procedures are required. Saving a user waveform to nonvolatile memory was discussed above on page 78.

Remote Programming

Introduction

The instrument may be remotely programmed via the GPIB interface, the RS-232 serial interface, or the LAN Ethernet interface. Any host computer interfaced to the instrument can easily control and monitor its operation.

Interface Configuration

All of the interface configuration parameters can be accessed via the front panel through shifted functions dedicated to the interface. Table 34 identifies the shifted functions that are used to configure each interface.

Table 34: Interface Configuration

Shifted Function	Interface Configuration
NET [•]	LAN, TCP/IP interface
GPIB [4]	GPIB 488.2 interface
RS-232 [5]	RS-232 serial interface

Each interface's configuration is accessed by pressing [SHIFT] followed by one of the interface keys ([NET], [GPIB], or [RS-232]). Once a given interface configuration is activated, parameters for the interface are selected by successive SELECT [▷] key presses. For example, pressing [SHIFT], [RS-232] activates the RS-232 configuration. The first menu item is RS-232 Enable/Disable. Pressing SELECT [▷] moves the selection to RS-232 baud rate.

Once a parameter is selected, it is modified by pressing the ADJUST [△] and [▽] keys. The only exception to this is for selections that require an internet address, such as static IP address, network mask, and default gateway address. In this case the address is modified by entering the new address with the numeric keys and pressing [ENTER].

All interfaces are enabled by default, but each interface may be disabled individually if desired. Any modifications made to an interface do not take effect until the interface is reset or the unit is power cycled.

GPIB

A GPIB (IEEE-488) communications port is included on the rear panel of the instrument. The instruments support the IEEE-488.1 (1978) interface standard. They also support the required common commands of the IEEE-488.2 (1987) standard.

The GPIB menu, [SHIFT] [4], enables the user to configure the GPIB remote interface. The GPIB menu has several options which are summarized in Table 35. Press the SELECT ◁ and ▷ keys to cycle through the options. Use the ADJUST △ and ▽ keys to change an option. Note that changes to the GPIB configuration do not take effect until the interface is reset or the instrument is power cycled.

Table 35: GPIB Menu Options

Parameter	Example Display	Description
GPIB	‘GPIB enabled’	Enable or disable all GPIB access
Address	‘Address 27’	GPIB address
Reset	‘Reset no’	Select ‘reset yes’ and press ‘ENTER’ to reset the GPIB interface.

GPIB Address

In order to communicate properly on the GPIB bus, the signal generator must be configured with a unique address. Use the Address menu option to set the unit’s GPIB address. Then reset the interface to make sure the new address is active.

Reset the GPIB Interface

Note that changes to the GPIB configuration do not take effect until the GPIB interface is either reset or the instrument is power cycled. To reset the GPIB interface, navigate through the GPIB menu options until “reset no” is displayed. Press the ADJUST △ key to display “reset yes” and press ENTER.

RS-232

An RS-232 communications port is included on the rear panel of the unit. The RS-232 interface connector is a standard 9 pin, type D, female connector configured as a DCE (transmit on pin 2, receive on pin 3). In order to communicate properly over RS-232, the instrument and the host computer both must be configured to use the same configuration. The following baud rates are supported: 115200 (default), 57600, 38400, 19200, 9600, and 4800. The rest of the communication parameters are fixed at 8 data bits, 1 stop bit, no parity, and RTS/CTS hardware flow control.

The RS-232 menu, [SHIFT] [5], has several options, which are summarized in Table 36. Press the SELECT ◁ and ▷ keys to cycle through the options. Use the ADJUST △ and ▽ keys to change an option. Note that changes to the RS-232 configuration do not take effect until the interface is reset or the instrument is power cycled.

Table 36: RS-232 Menu Options

Parameter	Example Display	Description
RS-232	'RS-232 enabled'	Enable or disable all RS-232 access
Baud rate	'Baud 11500'	The baud rate to use for RS-232 connections
Reset	'Reset no'	Select 'yes' and press 'ENTER' to reset the RS-232 interface.

RS-232 Configuration

Use the baud rate menu option to set the unit's baud rate. Then reset the interface to make sure the new baud rate is active.

Reset the RS-232 Interface

Note that changes to the RS-232 configuration do not take effect until the RS-232 interface is either reset or the instrument is power cycled. To reset the RS-232 interface, navigate through the RS-232 menu options until "reset no" is displayed. Press the ADJUST △ key display "reset yes" and press ENTER.

LAN

A rear panel RJ-45 connector may be used to connect the instrument to a 10/100 Base-T Ethernet LAN. Before connecting the instrument to your LAN, check with your network administrator for the proper method of configuration of networked instruments on your network.

The Ethernet LAN remote interface is configured via the NET menu, which has several options summarized in Table 37. Press the SELECT ◁ and ▷ keys to cycle through the options. Use the ADJUST △ and ▽ keys to change an option. Use the numeric keypad to enter an IP address when appropriate. Note that changes to the TCP/IP configuration do not take effect until the interface is reset or power is cycled.

Table 37: NET Menu Options for TCP/IP Configuration

Parameter	Example Display	Description
TCP/IP	'TCPIP enabled'	Enable or disable all TCP/IP access
DHCP	'DHCP enabled'	Enable or disable the DHCP client to automatically obtain an appropriate TCP/IP configuration from a DHCP server
Auto IP	'Auto IP enabled'	Enable or disable automatic network configuration in the 169.254.x.x internet address space if DHCP fails or is disabled.
Static IP	'Static enabled'	Enable or disable a static IP configuration.
IP	'IP 192.168.0.5'	IP address to use if static IP is enabled.
Subnet	'net 255.255.0.0'	Subnet mask to use if static IP is enabled.
Default gateway	'rtr 192.168.0.1'	Default gateway or router to use for routing packets not on the local network if static IP is enabled
Bare socket interface	'Bare enabled'	Enable or disable raw socket access on TCP/IP port 5025.
Telnet interface	'Telnet enabled'	Enable or disable telnet access on TCP/IP port 5024.
VXI-11 Interface	'Netinst enabled'	Enable or disable the VXI-11 net instrument remote interface.
Link speed	'Speed 100 Base-T'	Set the Ethernet link speed.
Reset	'Reset no'	Select 'Reset yes' and press 'ENTER' to reset the TCP/IP interface to use the latest TCP/IP configuration settings.

TCP/IP Configuration Methods

In order to function properly on an Ethernet based local area network (LAN), the unit needs to obtain a valid IP address, a subnet mask, and a default gateway or router address. There are three methods for obtaining these parameters: DHCP, Auto-IP, and Static IP. Check with your network administrator for the proper method of configuration of instruments on your network.

If the DHCP client is enabled, the unit will try to obtain its TCP/IP configuration from a DHCP server located somewhere on the local network. If the Auto-IP protocol is enabled, the unit will try to obtain a valid link-local IP configuration in the 169.254.x.x address space. If the static IP configuration is enabled, the unit will use the given TCP/IP configuration. When all three methods are enabled, the TCP/IP configuration will be determined in the following order of preference: DHCP, Auto-IP, and static IP. Given that Auto-IP is virtually guaranteed to succeed, it should be disabled if a static IP configuration is desired.

Please see the Status details on page 24 for details on viewing the TCP/IP address obtained via DHCP or Auto-IP methods.

TCP/IP Based Remote Interfaces

Three TCP/IP based remote interfaces are supported: raw socket, telnet, and VXI-11 net instrument. Raw socket access is available on port 5025. Telnet access is available on port 5024. The VXI-11 interface enables IEEE 488.2 GPIB-like access to the unit over TCP/IP. It enables controlled reads and writes and the ability to generate service requests. Most recent VISA instrument software libraries support this protocol.

Link Speed

The physical Ethernet layer supports 10 Base-T and 100 Base-T link speeds. The default link speed is set to 100 Base-T, but it can be set to 10 Base-T.

Reset the TCP/IP Interface

Note that changes to the TCP/IP configuration do not take effect until the TCP/IP interface is either reset or the instrument is power cycled. To reset the TCP/IP interface, navigate through the NET menu options until “reset no” is displayed. Press the ADJUST △ key to display “reset yes” and then press ENTER. Any active connections will be aborted. The TCP/IP stack will be re-initialized and configured using the latest configuration options.

Network Security

Network security is an important consideration for all TCP/IP networks. Please bear in mind that the unit does NOT provide security controls, such as passwords or encryption, for controlling access. If such controls are needed, you must provide it at a higher level on your network. This might be achieved, for example, by setting up a firewall and operating the instrument behind it.

Front-Panel Indicators

To assist in programming, there are three front panel indicators located under the INTERFACE section: REM, ACT, and ERR. The REM LED is on when the instrument is in remote lock out. In this mode, the front panel interface is locked out and the instrument can only be controlled via the remote interface. To go back to local mode, the user must press the LOCAL key, [3]. The ACT LED serves as an activity indicator that flashes every time a character is received or transmitted over one of the remote interfaces.

The ERR LED will be highlighted when a remote command fails to execute due to illegal syntax or invalid parameters. The user may view the cause of errors from the front panel by pressing the keys [SHIFT], [STATUS], sequentially. Next press ADJUST [△] until the display reads “Error Status”. Finally, press SELECT [▷] successively, to view the total error count followed by the individual errors. The error codes are described in section Error Codes on page 126.

Command Syntax

All commands use ASCII characters, are 4-characters long, and are case-insensitive. Standard IEEE-488.2 defined commands begin with the ‘*’ character followed by 3 letters. Instrument specific commands are composed of 4 letters.

The four letter mnemonic (shown in capital letters) in each command sequence specifies the command. The rest of the sequence consists of parameters.

Commands may take either *set* or *query* form, depending on whether the ‘?’ character follows the mnemonic. *Set only* commands are listed without the ‘?’, *query only* commands show the ‘?’ after the mnemonic, and *query optional* commands are marked with a ‘(?)’.

Parameters shown in { } and [ ] are not always required. Parameters in { } are required to set a value, and are omitted for queries. Parameters in [ ] are optional in both set and query commands. Parameters listed without any surrounding characters are always required.

Do NOT send () or {} or [] or spaces as part of the command.

The command buffer is limited to 768 bytes, with 25 byte buffers allocated to each of up to 3 parameters per command. If the command buffer overflows, both the input and output buffers will be flushed and reset. If a parameter buffer overflows, a command error will be generated and the offending command discarded.

Commands are terminated by a semicolon, a <CR> (ASCII 13), or a <LF> (ASCII 10). If the communications interface is GPIB, then the terminating character may optionally be accompanied by an EOI signal. If the EOI accompanies a character other than a <LF>, a <LF> will be appended to the command to terminate it. Execution of the command does not begin until a command terminator is received.

Aside from communication errors, commands may fail due to either syntax or execution errors. Syntax errors can be detected by looking at bit 5 (CME) of the event status register (*ESR?). Execution errors can be detected by looking at bit 4 (EXE) of the event status register. In both cases, an error code, indicating the specific cause of the error, is appended to the error queue. The error queue may be queried with the LERR? command. Descriptions of all error codes can be found in the section Error Codes, starting on page 126.

Parameter Conventions

The command descriptions use parameters, such as i, f, and v. These parameters represent integers or floating point values expected by the command. The parameters follow the conventions summarized in Table 38.

Table 38: Command Parameter Conventions

<table>
<tr><th>Parameter</th><th>Meaning</th></tr>
<tr><td>i, j, k</td><td>An integer value</td></tr>
<tr><td>d</td><td>A floating point value</td></tr>
<tr><td>f</td><td>A floating point value representing a frequency in Hz.</td></tr>
<tr><td>p</td><td>A floating point value representing a phase in degrees.</td></tr>
<tr><td>t</td><td>A floating point value representing time in seconds.</td></tr>
<tr><td>v</td><td>A floating point value representing voltage in volts.</td></tr>
<tr><td>u</td><td>An identifier of units. Allowed units depend on the type as identified below:
<table>
<tr><td>Type</td><td>Allowed Units</td></tr>
<tr><td>Amplitude</td><td>‘dBm’, ‘rms’, ‘Vpp’</td></tr>
<tr><td>Frequency</td><td>‘GHz’, ‘MHz’, ‘kHz’, or ‘Hz’</td></tr>
<tr><td>Time</td><td>‘ns’, ‘us’, ‘ms’, or ‘s’</td></tr>
</table></td></tr>
</table>

Numeric Conventions

Floating point values may be decimal (‘123.45’) or scientific (‘1.2345e2’). Integer values may be decimal (‘12345’) or hexadecimal (‘0x3039’).

Abridged Index of Commands

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Signal Synthesis Commands

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ALPH(?){d}	Page 105	α for Nyquist and Root-Nyquist Filters
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AWGN(?){i}	Page 105	Additive White Gaussian Noise
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WRTF i, <arb>	Page 115	Write User Filter
WRTW i, j, <arb>	Page 115	Write User Waveform

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REMT	Page 119	Go to Remote
UNLK?	Page 119	Release Lock
XTRM i{,j,k}	Page 119	Interface Terminator

Detailed Command List

Common IEEE-488.2 Commands

***CAL?** **Auto calibration**

This command currently does nothing and returns 0.

***CLS** **Clear Status**

Clear Status immediately clears the ESR and INSR registers as well as the LERR error buffer.

***ESE(?){i}** **Standard Event Status Enable**

Set (query) the Standard Event Status Enable register {to i}. Bits set in this register cause ESB (in STB) to be set when the corresponding bit is set in the ESR register.

***ESR?** **Standard Event Status Register**

Query the Standard Event Status Register. Upon executing a *ESR? query, the returned bits of the *ESR register are cleared. The bits in the ESR register have the following meaning:

Bit	Meaning
0	OPC – operation complete
1	Reserved
2	QYE – query error
3	DDE – device dependent error
4	EXE – execution error
5	CME – command error
6	Reserved
7	PON – power-on

Example

*ESR? A return of '176' would indicate that PON, CME, and EXE are set.

***IDN?** **Identification String**

Query the instrument identification string.

Example

*IDN? Returns a string similar to 'Stanford Research Systems,SG394,s/n004025,ver1.00.0B'

***OPC(?)** **Operation Complete**

The set form sets the OPC flag in the ESR register when all prior commands have completed. The query form returns '1' when all prior commands have completed, but does not affect the ESR register.

***PSC(?){i}** **Power-on Status Clear**

Set (query) the Power-on Status Clear flag {to i}. The Power-on Status Clear flag is stored in nonvolatile memory in the unit, and thus, maintains its value through power-cycle events.

If the value of the flag is 0, then the Service Request Enable and Standard Event Status Enable Registers (*SRE, *ESE) are stored in non-volatile memory, and retain their values through power-cycle events. If the value of the flag is 1, then these two registers are cleared upon power-cycle.

Example

*PSC 1	Set the Power-on Status Clear to 1.
*PSC?	Returns the current value of Power-on Status Clear.

***RCL i** **Recall Instrument Settings**

Recall instrument settings from location i. The parameter i may range from 0 to 9. Locations 1 to 9 are for arbitrary use. Location 0 is reserved for the recall of default instrument settings.

Example

*RCL 3	Recall instruments settings from location 3.

***RST** **Reset the Instrument**

Reset the instrument to default settings. This is equivalent to *RCL 0. It is also equivalent to pressing the keys [SHIFT], [INIT], [ENTER on the front panel. See Factory Default Settings on page 25 for a list of default settings.

Example

*RST	Resets the instrument to default settings

***SAV i** **Save Instrument Settings**

Save instrument settings to location i. The parameter i may range from 0 to 9. However, location 0 is reserved for current instrument settings. It will be overwritten after each front panel key press.

Example

*SAV 3	Save current settings to location 3.

***SRE(?){i}** **Service Request Enable**

Set (query) the Service Request Enable register {to i}. Bits set in this register cause the SG394 to generate a service request when the corresponding bit is set in the STB register.

***STB?** **Status Byte**

Query the standard IEEE 488.2 serial poll status byte. The bits in the STB register have the following meaning:

Bit	Meaning
0	INSB – INSR summary bit
1	Reserved
2	Reserved
3	Reserved
4	MAV – message available
5	ESB – ESR summary bit
6	MSS – master summary bit
7	Reserved

Example

*STB? A return of '113' would indicate that INSB, MAV, ESB, and MSS are set. INSB indicates that an enabled bit in INSR is set. MAV indicates that a message is available in the output queue. ESB indicates that an enabled bit in ESR is set. MSS reflects the fact that at least one of the summary enable bits is set and the instrument is requesting service.

***TRG** **Trigger**

When the instrument is configured for list operation, this command initiates a trigger. Instrument settings at the current list index are written to the instrument and the index is incremented to the next list entry.

***TST?** **Self Test**

Runs the instrument self test and returns 0 if successful. Otherwise it returns error code 17 to indicate that the self test failed. Use the LERR? command to determine the cause of the failure.

***WAI** **Wait for Command Execution**

The instrument will not process further commands until all prior commands including this one have completed.

Example

*WAI Wait for all prior commands to execute before continuing.

Status and Display Commands

DISP(?){i} — **Display**

Set (query) the current display value {to i}. The parameter i selects the display type.

i	Display
0	Modulation Type
1	Modulation Function
2	Frequency
3	Phase
4	Modulation Rate or Period
5	Modulation Deviation or Duty Cycle
6	RF Type N Amplitude
7	BNC Amplitude
10	BNC Offset
13	I Offset
14	Q Offset

Example

DISP 2 Show carrier frequency

INSE(?){i} — **Instrument Status Enable**

Set (query) the Instrument Status Enable register {to i}. Bits set in this register cause INSB (in STB) to be set when the corresponding bit is set in the INSR register.

INSR? — **Instrument Status Register**

Query the Instrument Status Register. Upon executing a INSR? query, the returned bits of the INSR register are cleared. The bits in the INSR register have the following meaning:

Bit	Meaning
0	20MHZ_UNLK – 20 MHz PLL unlocked.
1	100MHZ_UNLK – 100 MHz PLL unlocked.
2	19MHZ_UNLK – 19 MHz PLL unlocked.
3	1GHZ_UNLK – 1 GHz PLL unlocked.
4	4GHZ_UNLK – 4 GHz PLL unlocked.
5	NO_TIMEBASE – installed timebase is not oscillating.
6	RB_UNLOCK – the installed Rubidium oscillator is unlocked.
7	Reserved
8	MOD_OVLD – modulation overloaded.
9	IQ_OVLD – IQ modulation overloaded.
10-15	Reserved

Example

INSR? A return of ‘257’ would indicate that a modulation overload was detected and the 20 MHz PLL came unlocked.

LERR? **Last Error**

Query the last error in the error buffer. Upon executing a LERR? query, the returned error is removed from the error buffer. See the section Error Codes later in this chapter for a description of the possible error codes returned by LERR?. The error buffer has space to store up to 20 errors. If more than 19 errors occur without being queried, the 20^{th} error will be 254 (Too Many Errors), indicating that errors were dropped.

OPTN? i **Installed Options**

Query whether option i is installed. Returns 1 if it is installed, otherwise 0. The parameter i identifies the option.

i	Option
1	Rear clock outputs (never installed)
2	RF doubler and DC outputs (never installed)
3	IQ modulation inputs and outputs (always installed)
4	Rubidium timebase

ORNG? [i] **Output Over Range**

Query whether output i is over its specified range. The instrument returns one if the given output is over range, otherwise 0. The parameter i identifies the output as follows:

i	Output
0	BNC output
1	Type N outputs

If omitted, i defaults to 1.

TEMP? **Temperature**

Query the current temperature of the RF output block in degrees C.

TIMB? **Timebase**

Query the current timebase. The returned value identifies the timebase.

Value	Meaning
0	Crystal timebase
1	OCXO timebase
2	Rubidium timebase
3	External timebase

Signal Synthesis Commands

Signal synthesis commands enable the user to set the frequency, amplitude, and phase of the outputs. Basic configuration can be achieved by following the steps as outlined in Table 39.

Table 39: Basic Signal Configuration

Action	Relevant Commands
Set frequency	FREQ
Set amplitude	AMPL, AMPR
Set offset	OFSL
Adjust phase	PHAS, RPHS

All of these commands are described in detail below.

AMPL(?){v}[u] **Amplitude of LF (BNC Output)**

Set (query) the amplitude of the low frequency BNC output {to v}. If omitted, units default to dBm.

Example

AMPL -1.0	Set the BNC output amplitude to –1.0 dBm.
AMPL 0.1 RMS	Set the BNC output amplitude to 0.1 V_{rms}.
AMPL?	Query the BNC output amplitude in dBm.

AMPR(?){v}[u] **Amplitude of RF (Type N Output)**

Set (query) the amplitude of the Type N RF output {to v}. If omitted, units default to dBm.

Example

AMPR -3.0	Set the Type N RF output amplitude to –3.0 dBm.
AMPR 0.1 RMS	Set the Type N RF output amplitude to 0.1 V_{rms}.
AMPR?	Query the Type N RF output amplitude in dBm.

ENBL(?){i} **Enable LF (BNC Output)**

Set (query) the enable state of the low frequency BNC output {to i}. If i is 0, the output is disabled and turned off. If i is 1, the output is enabled and operating at the programmed amplitude for the output. Note that the query returns the current state of the output. It may return 0 even if a 1 was sent if the output is not active at the current frequency (i.e. $F_{carrier} > 62.5$ MHz).

ENBR(?){i} **Enable RF (Type N Output)**

Set (query) the enable state of the Type N RF output {to i}. If i is 0, the output is disabled and turned off. If i is 1, the output is enabled and operating at the programmed amplitude for the output. Note that the query returns the current state of the output. It may return 0 even if a 1 was sent if the output is not active at the current frequency (i.e. $F_{carrier} < 950$ kHz).

FREQ(?){f}[u] **Frequency**

Set (query) the carrier frequency {to f}. If omitted, units default to Hz.

Example

FREQ 100e6	Set the frequency to 100 MHz.
FREQ 100 MHz	Also sets the frequency to 100 MHz.
FREQ ?	Returns the current frequency in Hz.
FREQ? MHz	Returns the current frequency in MHz

NOIS(?){i} **Noise Mode of RF PLL Loop Filter**

Set (query) the RF PLL loop filter mode for the instrument.

i	RF PLL Mode
0	Mode 1—minimize noise at small offsets from carrier.
1	Mode 2—minimize noise at large offsets from carrier.

This command is identical to changing the PLL mode from the front panel via the shifted CAL function.

OFSL(?){v} **Offset of LF (BNC Output)**

Set (query) the offset voltage of the low frequency BNC output {to v} in volts.

PHAS(?){p} **Phase**

Set (query) the phase of the carrier{to p}. The phase will track to ±360°, but it may only be stepped by 360° in one step. Thus, if the phase is currently 360°, setting the phase to –90° will fail because the phase step is larger than 360°. On the other hand, setting the phase to 370° will succeed but the reported phase will then be 10°.

Example

PHAS 90.0	Set the phase to 90 degrees.
PHAS -10.0	Set the phase to –10 degrees.

RPHS **Rel Phase**

Make the current phase of the carrier 0°.

Modulation Commands

Modulation commands enable the user to configure different types of modulation of the carrier. Basic configuration for analog modulation can be achieved by following the steps outlined in Table 40.

Table 40: Basic Analog Modulation Configuration

Modulation	Configuration	Relevant Commands
On/Off	Enable modulation	MODL
External	AC/DC input coupling	COUP
AM	Select AM modulation	TYPE 0, STYP 0
	Modulation function	MFNC
	Mod. rate / Noise bandwidth	RATE
	Deviation	ADEP, ANDP
FM	Select FM modulation	TYPE 1, STYP 0
	Modulation function	MFNC
	Mod. rate / Noise bandwidth	RATE
	Deviation	FDEV, FNDV
ΦM	Select ΦM modulation	TYPE 2, STYP 0
	Modulation function	MFNC
	Mod. rate / Noise bandwidth	RATE
	Deviation	PDEV, PNDV
Sweep	Select frequency sweep	TYPE 3
	Modulation function	SFNC
	Modulation rate	SRAT
	Deviation	SDEV
Pulse/Blank	Select pulse/blank mod.	TYPE 4/TYPE 5
	Modulation function	PFNC
	Pulse period	PPER
	Pulse width	PWID or PDTY
	PRBS period	RPER
	PRBS length	PRBS

The remote interface commands associated with each setting are shown in the table. Analog modulation is indicated by setting the subtype to zero (STYP command). Modulation type is selected via the TYPE command. Although not shown, analog modulation also supports user waveforms downloaded by the user. This is achieved by setting the modulation function (MFNC, SFNC, or PFNC) to user waveform and selecting the desired user waveform via the WAVF command. All of these commands are described in detail below.

Basic configuration for digital vector modulation can be achieved by following the steps outlined in Table 41.

Table 41: Basic Vector Modulation Configuration

Modulation	Configuration	Relevant Commands
On/Off	Enable modulation	MODL
ASK	Select AM modulation	TYPE 0
	Select constellation	STYP, CNST
	Modulation function	QFNC, WAVF
	Pulse shaping filter	FLTR, ALPH, BTEE
	Symbol rate	SYMR
FSK	Select FM modulation	TYPE 1
	Select constellation	STYP, CNST
	Modulation function	QFNC, WAVF
	Pulse shaping filter	FLTR, ALPH, BTEE
	Symbol rate	SYMR
	Deviation	FDEV
ΦM	Select ΦM modulation	TYPE 2
	Select constellation	STYP, CNST
	Modulation function	QFNC, WAVF
	Pulse shaping filter	FLTR, ALPH, BTEE
	Symbol rate	SYMR
QAM	Select QAM modulation	TYPE 7
	Select constellation	STYP, CNST
	Modulation function	QFNC, WAVF
	Pulse shaping filter	FLTR, ALPH, BTEE
	Symbol rate	SYMR
CPM	Select CPM modulation	TYPE 8
	Select constellation	STYP
	Modulation function	QFNC, WAVF
	Pulse shaping filter	FLTR, ALPH, BTEE
	Symbol rate	SYMR
	Modulation index	MODI
VSB	Select VSB modulation	TYPE 9
	Select constellation	STYP
	Modulation function	QFNC, WAVF
	Pulse shaping filter	FLTR, ALPH, BTEE
	Symbol rate	SYMR

The remote interface commands associated with each setting are shown in the table. In contrast to analog modulation, digital vector modulation involves the mapping of digital symbols onto a vector constellation. Thus, instead of a waveform frequency or period, we have a symbol rate (SYMR command). The digital symbols are also typically played back through pulse shaping filter characterized via the FLTR command. All of these commands are described in detail below.

ADEP(?){d}

AM Modulation Depth

Set (query) the AM modulation depth {to d} in percent.

Note: see ANDP command if noise is the selected modulation function.

Example

ADEP 90.0	Set the depth to 90 %.
ADEP?	Query the current depth in percent.

ALPH(?){d}

α for Nyquist and Root-Nyquist Filters

Set (query) the excess bandwidth factor, α, for Nyquist and Root-Nyquist filters {to d}. It may range from 0.1 to 1.0.

Example

ALPH 0.2	Set α to 0.2.
ALPH?	Query the current value for α

ANDP(?){d}

AM Noise Modulation Depth

Set (query) the AM noise modulation depth {to d} in percent. The value controls the rms depth of the modulation, not the peak deviation as the ADEP command does.

Note: see ADEP command for all modulation functions other than noise.

Example

ANDP 10.0	Set the rms noise depth to 10 %.
ANDP?	Query the current rms noise depth in percent.

AWGN(?){i}

Additive White Gaussian Noise

Set (query) the current configuration for AWGN {to i}. The parameter i may be set to one of the following values:

i	Configuration
0	Noise Off
1	Noise Added
2	Noise Only

Note: see NPWR to configure the noise power.

BITS?

Bits/Symbol for Constellation

Query the current bits/symbol for the current constellation. Bits/symbol is set by the selected constellation. If constellations are not used it will be 16 or 32. The latter value is for IQ waveforms that contain 16-bit IQ value pairs.

BTEE(?){d}

BT for Gaussian Filters

Set (query) the current bandwidth, symbol time product, BT, for Gaussian filters to {d}. It may range from 0.1 to 1.0.

Example

BTEE 0.3	Set BT to 0.3.
BTEE?	Query the current value for α

CATL?

Catalog Listing of User Waveforms

Query the current catalog listing of available user waveforms. The commands returns a comma separated list of location and waveform size in 16-bit words.

When all waveforms have been itemized, the current free space in 16-bit words for new waveforms is appended to the list.

Example

CATL?	Query the current catalog listing. An example response might be the following:

0,512,1,0,2,128,3,0,4,0,5,0,6,0,7,0,8,0,9,0,10,173696,11,720,12,128,13,79,14,235,15,76800,1044480

In this example, SRAM has a waveform 512 words long. Location 2 has a waveform 128 words long. All other user waveforms are empty. Locations 10 to 14 indicate the presence of factory loaded read-only waveforms (see WAVF for details). Finally the last number indicates we have 1,044,480 words of free space still available for storage of new waveforms in nonvolatile memory.

CNST(?){i} **User Constellation**

Set (query) the current user constellation {to i}. The parameter i may range from 0 to 9. The value, 0, identifies the constellation stored in SRAM. Values 1 to 9 identify user constellations stored in nonvolatile memory via the SAVC command. Note that user constellations are only active when the modulation subtype is user (see STYP command).

COUP(?){i} **Modulation Coupling**

Set (query) the coupling of the external modulation input {to i}. If i is 0, the input is AC coupled. If i is 1, the input is DC coupled. This setting has no affect on the input if pulse modulation is active. In that case the coupling is always DC.

DELW? i **Delete User Waveform**

Delete the user waveform at location i and return an error code followed by the current free space in nonvolatile memory in 16-bit words. The parameter i may range from 0 to 9. The value, 0, identifies any waveform stored in SRAM. Values 1 to 9 identify waveforms stored in nonvolatile memory via the SAVW command. If successful, the error code will be 0. Note that factory loaded, read-only waveforms cannot be deleted with this command.

WARNING: once deleted, a user waveform cannot be recovered.

ERAS? **Erase All User Waveforms**

Erase all user waveforms and return an error code followed by the current free space in nonvolatile memory in 16-bit words. If successful, the error code will be 0. Note that factory loaded, read-only waveforms cannot be deleted by this command.

WARNING: once deleted, user waveforms cannot be recovered.

FDEV(?){f}[u] **FM Deviation**

Set (query) the FM deviation {to f}. If omitted, units default to Hz.

Note: see FNDV command if noise is the selected modulation function.

Example

FDEV 10e3	Set the FM deviation to 10 kHz.
FDEV?	Query the current FM deviation in Hz.
FDEV 1 kHz	Set the FM deviation to 1 kHz.

FLTR(?){i} **Pulse Shaping Filter**

Set (query) the current pulse shaping filter {to i}. The parameter i identifies the pulse shaping filter. It may be set to one of the following values:

i	Filter
0	User filter stored in SRAM
1–9	User filters stored in nonvolatile memory
10	Nyquist (raised cosine) filter
11	Root-Nyquist (root-raised cosine) filter
12	Gaussian filter
13	Rectangular filter
14	Triangular filter (simple, linear interpolation)
15	Kaiser windowed sinc filter.
16	Linearized Gaussian filter (used in GSM EDGE modulation)
17	C4FM (used in APCO 25 modulation)

For Nyquist and Root-Nyquist filters, see the ALPH command to set the excess bandwidth factor, α. For the Gaussian filter, see the BTEE command to set the bandwidth, symbol time product, BT.

Example

FLTR 10	Set pulse shaping filter to raised cosine.
ALPH 0.3	Set α for raised cosine filter to 0.3

FNDV(?){f}[u] **FM Noise Deviation**

Set (query) the FM noise deviation {to f}. If omitted, units default to Hz. The value controls the rms deviation of the modulation, not the peak deviation as the FDEV command does.

Note: see FDEV command for all modulation functions other then noise.

Example

FNDV 10e3	Set the rms FM noise deviation to 10 kHz.
FNDV?	Query the current rms FM noise deviation in Hz.
FNDV 1 kHz	Set the rms FM noise deviation to 1 kHz.

MFNC(?){i} **Modulation Function for Analog AM/FM/ΦM**

Set (query) the modulation function or AM/FM/ΦM {to i}. The parameter i may be set to one of the following values:

i	Modulation Function
0	Sine wave
1	Ramp
2	Triangle
3	Square
4	Noise
5	External
11	User waveform

Note: see SFNC, PFNC, and QFNC commands for sweeps, pulse/blank, and IQ modulations respectively.

MODI(?){d} **Modulation Index for CPM**

Set (query) the modulation index for CPM {to d}. The modulation index may range from 0.0 to 1.0. The modulation index is stored as a 3 digit floating point decimal. However, when applied to the modulation, it will be rounded to the nearest rational factor, n/512, where n is an integer.

Example

MODI 0.5	Set modulation index to 1/2.
MODI 0.438	Set modulation index to 7/16.
MODI?	Query the current modulation index

MODL(?){i} **Modulation Enable**

Set (query) the enable state of modulation {to i}. If i is 0, modulation is disabled. If i is 1, modulation is enabled. This command may fail if the current modulation type is not allowed at current settings. For example, pulse modulation is not allowed at frequencies where the RF doubler is active.

MPRE i **Modulation Preset**

Configure the instrument according to the given modulation preset. The parameter i identifies the modulation preset, which may be one of the following values:

i	Modulation Preset
0	AM audio clip
1	FM audio clip
2	NADC modulation
3	PDC modulation
4	DECT frame
5	APCO 25 modulation
6	TETRA modulation
7	GSM frame
8	GSM EDGE frame
9	W-CDMA frame
10	ATSC DTV modulation

This command is identical to executing the front panel shifted function for modulation presets: [SHIFT] [FREQ].

Example

MPRE 8	Setup the instrument to modulate a frame of GSM EDGE.
MODL 1	Enable the modulation

NPWR(?){d} **Noise Power**

Set (query) the current AWGN power {to d} in dB. The noise power may range from -10.0 to -70 dB.

Note: see command AWGN for configuring whether noise is to be added to a modulation.

Example

NPWR –30.0	Set noise power to –30.0 dB
AWGN 1	Add noise to current modulation

OFSI(?){d} **Offset for I in IQ Modulation**

Set (query) the current offset for I in IQ modulation to {to d} in percent. The offset may range from –5.0 to +5.0%. Note that IQ offsets only apply to internally generated IQ waveforms.

Example

OFSI 0.5	Set the offset for I to 0.5%
OFSI –1.5	Set the offset for I to –1.5%

OFSQ(?){d} **Offset for Q in IQ Modulation**

Set (query) the current offset for Q in IQ modulation to {to d} in percent. The offset may range from –5.0 to +5.0%.Note that IQ offsets only apply to internally generated IQ waveforms.

Example

OFSQ 0.5	Set the offset for Q to 0.5%
OFSQ –1.5	Set the offset for Q to –1.5%

PDEV(?){p} **ΦM Deviation**

Set (query) the ΦM deviation {to p} in degrees.

Note: see PNDV command if noise is the selected modulation function.

Example

PDEV 45.0	Set the ΦM deviation to 45.0 degrees.
PDEV?	Query the current ΦM deviation.

PDTY(?){d} **Pulse/Blank Duty Factor**

Set (query) the duty factor for pulse/blank modulation {to d} in percent. This value controls pulse modulation when the selected waveform is square (see PFNC). Use PWID? to determine the actual pulse width in time.

Example

PDTY 10	Set the duty factor to 10 %.
PDTY?	Query the current duty factor.

PFNC(?){i} **Pulse Modulation Function**

Set (query) the modulation function for pulse/blank modulation {to i}. The parameter i may be set to one of the following values:

i	Modulation Function
3	Square
4	Noise (PRBS)
5	External
11	User waveform

Note: see MFNC, SFNC, and QFNC commands for AM/FM/ΦM, sweeps, and IQ modulations respectively.

PNDV(?){p} **ΦM Noise Deviation**

Set (query) the ΦM noise deviation {to p} in degrees. The value controls the rms deviation of the modulation, not the peak deviation as the PDEV command does.

Note: see PDEV command for all modulation functions other than noise.

Example

PNDV 10.0	Set the rms ΦM noise deviation to 10.0 degrees.
PNDV?	Query the current rms ΦM noise deviation.

PPER(?){t}[u] **Pulse/Blank Period**

Set (query) the pulse/blank modulation period {to t}. If omitted, units default to seconds. This value controls pulse modulation when the selected waveform is square (see PFNC).

Example

PPER 1e-3	Set the pulse period to 1 ms.
PPER?	Query the current pulse period in seconds.

PRBS(?){i} **PRBS Length for Pulse/Blank Modulation**

Set (query) the PRBS length for pulse/blank modulation {to i}. The parameter i may range from 5 to 32. It defines the number of bits in the PRBS generator. A value of 8, for example, means the generator is 8 bits wide. It will generate a sequence of pseudo random bits which repeats every $2^8 – 1$ bits. This value controls pulse modulation when the selected waveform is noise (see PFNC).

Example

PRBS 10	Set the PRBS length to 10.
PRBS?	Query the current PRBS length.

PTRN(?){i} **Pattern Data**

Set (query) the 16-bit data word for pattern waveforms {to i}.

Example

PTRN 0x1E1E	Set the current 16-bit data word to 0x1E1E in hex.
PTRN?	Query the current 16-bit data word.

PWID(?){t}[u] **Pulse/Blank Width**

Set (query) the pulse/blank modulation width (duty cycle) {to t}. If omitted, units default to seconds. This value controls pulse modulation when the selected waveform is square (see PFNC).

Example

PWID 1e-6	Set the pulse width to 1 μs.
PWID?	Query the current pulse width in seconds.

QFNC(?){i} **IQ Modulation Function**

Set (query) the modulation function for IQ modulation {to i}. The parameter i may be set to one of the following values:

i	Modulation Function
0	Sine
1	Ramp
2	Triangle
3	Square
4	Phase noise

5	External
6	Sine/Cosine
7	Cosine/Sine
8	IQ Noise
9	PRBS symbols
10	Pattern (16 bits)
11	User waveform

Not all values are valid in all modulation modes.

Note: see MFNC, SFNC, and PFNC commands for AM/FM/ΦM, sweeps, and pulse/blank modulations respectively.

RATE(?){f}[u] **Modulation Rate for AM/FM/ΦM**

Set (query) the modulation rate {to f}. If omitted, units default to Hz. This command also controls the noise bandwidth if a noise function is selected for the given type of modulation.

Note: use the SRAT command to control sweep rates and SYMR to control the symbol rate of user waveforms.

Example

RATE 400	Set the modulation rate to 400 Hz.
RATE 10 kHz	Set the rate to 10 kHz.
RATE?	Query the current rate in Hz.
RATE? kHz	Query the current rate in kHz.

RPER(?){t}[u] **PRBS Period for Pulse/Blank Modulation**

Set (query) the PRBS period for pulse/blank modulation{to t}. If omitted, units default to seconds. This value controls pulse modulation when the selected waveform is noise (see PFNC).

Example

RPER 1e-3	Set the bit period to 1 ms.
RPER?	Query the current bit period in seconds.

SAVC? i **Save User Constellation**

Save the user constellation stored in SRAM to location i in nonvolatile memory and return an error code when complete. If successful, the error code will be 0. The location may be an integer from 1 to 9.

Example

SAVC? 3	Save the current constellation in SRAM to location 3 in nonvolatile memory.

SAVF? i **Save User Filter**

Save the user filter stored in SRAM to location i in nonvolatile memory and return an error code when complete. If successful, the error code will be 0. The location may be an integer from 1 to 9.

Example

SAVF? 2	Save the current filter in SRAM to location 2 in nonvolatile memory.

SAVW? i — **Save User Waveform**

Save the user waveform stored in SRAM to location i in nonvolatile memory. When complete, return an error code, followed by the current free space in nonvolatile memory in 16-bit words. If successful, the error code will be 0. Refer to the section Error Codes on page 126 for all other error codes.

Example

SAVW? 1	Save the current filter in SRAM to location 1 in nonvolatile memory. An example response might be

0,1044480

In this example, the returned error code was 0 indicating success. Furthermore, after the waveform was saved, there were 1,044,480 words of free space available in nonvolatile memory for new waveforms.

SCAL(?){d} — **Scale Waveform**

Set (query) the digital scale factor for modulation waveforms {to d}. The scale factor may range from 0.2 to 3.0. The digital scale factor enables the user to adjust the amplitude of the modulation waveform digitally. This factor applies to IQ modulation waveforms that vary the amplitude, such as ASK, PSK, and QAM, but not to constant amplitude waveforms, such as FM and CPM. As the scale factor is increased, the amplitude of the waveform is increased, but the likelihood that the waveform will be clipped is also increased. As the scale factor is decreased, the amplitude of the waveform will be decreased, but it will also be more susceptible to quantization noise. This parameter should normally be left at 1.0.

SDEV(?){f}[u] — **Sweep Deviation**

Set (query) the deviation for sweeps {to f}. If omitted, units default to Hz. The limits for sweep deviations are controlled by the edges of the band within which the synthesizer is operating. Sweep deviations may be as large as 1 GHz in the 2 to 4 GHz band.

Example

SDEV 100e6	Set the sweep deviation to 100 MHz.
SDEV?	Query the current sweep deviation in Hz.
SDEV 1 MHz	Set the sweep deviation to 1 MHz.

SFNC(?){i} — **Sweep Modulation Function**

Set (query) the modulation function for sweeps {to i}. The parameter i may be set to one of the following values:

i	Modulation Function
0	Sine wave
1	Ramp
2	Triangle
5	External
11	User waveform

Note: see MFNC, PFNC, and QFNC commands for AM/FM/ΦM, pulse/blank, and IQ modulations respectively.

SRAT(?){f}[u] **Modulation Sweep Rate**

Set (query) the modulation rate for sweeps {to f}. If omitted, units default to Hz.

Note: use the RATE command to control the modulation rate of AM/FM/ ΦM.

Example

SRAT 10	Set the sweep rate to 10 Hz.
SRAT?	Query the current rate in Hz.

STAG? **Staggered Constellation**

Query whether the current constellation operates in staggered mode. The command returns 1 if staggered mode is enabled, otherwise, it returns 0.

STYP(?){i} **Modulation Subtype**

Set (query) the modulation subtype {to i}. The parameter i may be set to one of the following values:

i	Modulation Subtype
0	Analog (no constellation mapping)
1	Vector (no constellation mapping)
2	Default 1-bit constellation
3	Default 2-bit constellation
4	Default 3-bit constellation
5	Default 4-bit constellation
6	Default 5-bit constellation
7	Default 6-bit constellation
8	Default 7-bit constellation
9	Default 8-bit constellation
10	Default 9-bit constellation
11	User constellation
12	Factory OQPSK constellation
13	Factory DQPSK constellation
14	Factory π/4 DQPSK constellation
15	Factory 3π/8 8PSK constellation

Example

STYP 3	Select default 2-bit vector modulation
STYP?	Query the current modulation subtype.

Note that not all modulation subtypes are valid for each modulation type. Allowed subtypes for each type of modulation are summarized in Table 42.

Table 42: Allowed subtypes for each type of modulation

Modulation Type	Allowed Subtypes
AM/ASK	0-5, 11
FM/FSK	0-5, 11
PM/PSK	0-5, 11-15
Sweep	0
Pulse/Blank	0
QAM	3, 5-7, 9, 11
CPM	2-5
VSB	4-5

SYMR(?){f}[u] **Symbol Rate for Digital Waveforms**

Set (query) the symbol rate for digital waveforms {to f}. If omitted, units default to Hz.

Note: use the RATE and SRAT commands to control modulation rates for functional waveforms in AM/FM/ΦM and sweeps.

Example

SYMR 270.833e3	Set the symbol rate to 270.833 kHz.
SYMR 10 kHz	Set the symbol rate to 10 kHz.
SYMR?	Query the current rate in Hz.
SYMR? kHz	Query the current rate in kHz.

TDMA? **Current TDMA Configuration**

Query the current TDMA configuration word. The TDMA configuration word is described in the section TDMA, starting on page 84

Example

TDMA?	Query the current TDMA configuration. An example response might be

197121

In hexadecimal format this number is 0x00030201. Referring to the definition of the TDMA configuration word, bit 0 indicates that TDMA is enabled; bits 11-8 indicate a ramp period of 2 symbols; and bits 17-16 indicate that the RF power is controlled by event marker #3.

TYPE(?){i} **Modulation Type**

Set (query) the current modulation type {to i}. The parameter i may be set to one of the following values:

i	Modulation Type
0	AM/ASK
1	FM/FSK
2	ΦM/PSK
3	Sweep
4	Pulse
5	Blank
7	QAM
8	CPM
9	VSB

Example

TYPE 2	Set the modulation type to phase modulation.

Note that the modulation subtype, STYP, must also be specified to fully configure the modulation.

WAVF(?){i} **User Waveform**

Set (query) the current user waveform {to i}. The parameter i identifies the desired user waveform. It may be one of the following values:

i	User Waveform
0	User waveform stored in SRAM
1–9	User waveforms stored in nonvolatile memory
10	Audio clip
11	DECT frame of random data
12	TETRA frame of random data
13	GSM frame of random data
14	GSM EDGE frame of random data
15	W-CDMA mobile station frame of random data

Note that the user waveform is only active when the modulation function is set to user waveform (11). See MFNC, SFNC, PFNC, and QFNC. The value –1 is returned if the current waveform is invalid. This might happen, for instance, if the waveform has been deleted. Values 10 and above refer to read-only waveforms loaded at the factory. These are typically configured as a consequence of modulation preset execution (MPRE command).

Example

WAVF 2 — Select user waveform 2 for modulation

WRTC i, j, <arb data> — **Write User Constellation**

Write the given user constellation to SRAM. The parameter i identifies the bits/symbol for the constellation. It may be 1 to 9, 16, or 32. Parameter j indicates whether the constellation uses staggered IQ mode or not. Staggered mode is indicated if j = 1. Otherwise j = 0. The <arb data> is a definite arbitrary block of binary data defining the constellation. See section User Constellations starting on page 79 for details on how to construct the <arb data> block.

WRTE i, <arb data> — **Write Event Marker Configuration**

Write the given event marker configuration to SRAM. The parameter i identifies the TDMA configuration word to apply to the constellation. The TDMA configuration word is described in the section TDMA, starting on page 84. The <arb data> is a definite arbitrary block of binary data defining the event marker configuration. See section Event Markers and TDMA starting on page 84 for details on how to construct the <arb data> block.

WRTF i, <arb data> — **Write User Filter**

Write the given filter to SRAM. The parameter i identifies the offset to apply to each coefficient of the filter. The <arb data> is a definite arbitrary block of binary data defining the filter coefficients. See section User Filters starting on page 82 for details on how to construct the <arb data> block.

WRTW i, j, <arb data> — **Write User Waveform**

Write the given user waveform to SRAM. The parameter i identifies the bits/symbol and whether it is an analog or vector waveform. The parameter j indicates the number of bits in the waveform. The <arb data> is a definite arbitrary block of binary data defining the waveform. See section Arbitrary User Waveforms starting on page 76 for details on how to construct the <arb data> block.

List Commands

For detailed information on creating and defining lists, see the section List Mode later in this chapter. Basic steps for using lists are summarized in Table 43.

Table 43: Basic List Configuration

Action	Relevant Commands
Create list	LSTC
Set instrument state for each list entry	LSTP
Enable list	LSTE
Trigger list	*TRG or GPIB bus trigger
Delete list	LSTD

All of these commands are described in detail below.

LSTC? i **List Create**

Create a list of size i. If successful, 1 is returned, otherwise 0 is returned. The list is initialized to the no change state.

Example

LSTC? 20 Create a list of size 20. Returns 1 if successful, otherwise 0.

LSTD **List Delete**

Delete the current list and free any memory dedicated to it.

Example

LSTD Destroy a previously created list.

LSTE(?){i} **List Enable**

Set (query) the list enable state {to i}. If i is 1, the list is enabled. If i is 0 it is disabled. A list must be enabled before it can be triggered.

Example

LSTE 1 Enable a previously created list.
LSTE? Query the current enable state of the list.

LSTI(?){i} **List Index**

Set (query) the current list index pointer {to i}.The list index identifies the entry whose state will be loaded into the instrument upon the next valid trigger.

Example

LSTI 10 Set the list index to 10.
LSTI? Query the current list index.

LSTP(?) i {,<st>} **List Point**

Set (query) the instrument state stored in entry i of the list {to <st>}. Details on the format and meaning of instrument states <st> are discussed above in the section List Instrument States.

Example

LSTP 5, 100e6,N,N,N,N,N,N,N,N,N,N,N,N,N,N,N
Set list entry 5 in the list to change the frequency to 100 MHz but leave all other settings unchanged.
LSTP? 5 Query instrument state stored in list entry 5.

LSTR	List Reset
	Reset the list index to zero.

LSTS?	List Size
	Query the current list size. This is the size requested when the list was created with the LSTC? command.

Interface Commands

EMAC? **Ethernet MAC Address**

Query the Ethernet MAC address.

EPHY(?){i} **Ethernet Physical Layer Configuration**

Set (query) the Ethernet link speed {to i}. The parameter i may be one of the following:

i	Link Speed
0	10 Base T
1	100 Base T

Example

EPHYS 1	Configure link for 100 Base T operation.

IFCF(?)i{,j} **Interface Configuration**

Set (query) interface configuration parameter i {to j}. The parameter i may be one of the following:

i	Configuration Parameter
0	RS-232 Enable/Disable
1	RS-232 Baud Rate
2	GPIB Enable/Disable
3	GPIB Address
4	LAN TCP/IP Enable/Disable.
5	DHCP Enable/Disable
6	Auto-IP Enable/Disable
7	Static IP Enable/Disable
8	Bare Socket Enable/Disable
9	Telnet Enable/Disable
10	VXI-11 Net Instrument Enable/Disable
11	Static IP Address
12	Subnet Address/Network Mask
13	Default Gateway

Set j to 0 to disable a setting and 1 to enable it. Valid RS-232 baud rates include 4800, 9600, 19200, 38400, 57600, and 115200. Valid GPIB addresses are in the range 0–30. Parameters 10–12 require an IP address in the form ‘a.b.c.d’ where each letter is a decimal integer in the range 0–255.

Example

IFCF 6,0	Disable Auto-IP
IFCF 1,19200	Set RS-232 baud rate to 19200
IFCF 3,16	Set primary GPIB address to 16
IFCF 11,192.168.10.5	Set IP address to 192.168.10.5
IFCF 12,255.255.255.0	Set network mask to 255.255.255.0
IFCF 13,192.168.10.1	Set default gateway to 192.168.10.1

IFRS i — **Interface Reset**

Reset interface i. The parameter i identifies the interface to reset:

i	Interface
0	RS-232
1	GPIB
2	LAN TCP/IP

When an interface is reset all connections on that interface are reset to the power-on state.

IPCF? i — **Active TCP/IP Configuration**

Query active TCP/IP configuration parameter i. The parameter i may be one of the following:

i	Configuration
0	Link
1	IP Address
2	Subnet Address/Network Mask
3	Default Gateway

The link parameter indicates whether the unit is physically connected to the LAN/Ethernet network. A value of 1 indicates the unit is connected. The rest of the parameters indicate the current TCP/IP configuration that was selected by the appropriate configuration process: DHCP, Auto-IP, or Static IP.

LCAL — **Go to Local**

Go back to local control of the instrument. This enables the front panel key pad for instrument control. This command is only active on raw socket, telnet and RS-232 connections. The other interfaces have built in functionality for implementing this functionality.

LOCK? — **Request Lock**

Request the instrument lock. The unit returns 1 if the lock is granted and 0 otherwise. When the lock is granted, no other instrument interface, including the front panel interface, may alter instrument settings until the lock is released via the UNLK command.

REMT — **Go to Remote**

Enable remote control of the instrument. In this mode, the front panel key pad is disabled, so that control of the instrument can only occur via the remote interface. This command is only active on raw socket, telnet and RS-232 connections. The other interfaces have built in functionality for implementing this functionality.

UNLK? — **Release Lock**

Release the instrument lock previously acquired by the LOCK? command. Returns 1 if the lock was released, otherwise 0.

XTRM i{,j,k} — **Interface Terminator**

Set the interface terminator that is appended to each response to i, j, k.
The default terminator is 13, 10, which is a carriage return followed by a line feed.

Status Byte Definitions

The instrument reports on its status by means of the serial poll status byte and two event status registers: the standard event status (*ESR) and the instrument event status (INSR). These read-only registers record the occurrence of defined events inside the unit. If the event occurs, the corresponding bit is set to one. Bits in the status registers are latched. Once an event bit is set, subsequent state changes do not clear the bit. All bits are cleared when the registers are queried, with a *ESR?, for example. The bits are also cleared with the clear status command, *CLS. The bits are not cleared, however, with an instrument reset (*RST) or a device clear.

Each of the unit's event status registers has an associated enable register. The enable registers control the reporting of events in the serial poll status byte (*STB). If a bit in the event status register is set and its corresponding bit in the enable register is set, then the summary bit in the serial poll status byte (*STB) will be set. The enable registers are readable and writable. Reading the enable registers or clearing the status registers does not clear the enable registers. Bits in the enable registers must be set or cleared explicitly. To set bits in the enable registers, write an integer value equal to the binary weighted sum of the bits you wish to set.

The serial poll status byte (*STB) also has an associated enable register called the service request enable register (*SRE). This register functions in a similar manner to the other enable registers, except that it controls the setting of the master summary bit (bit 6) of the serial poll status byte. It also controls whether the unit will issue a request for service on the GPIB bus.

Serial Poll Status Byte

Bit	Name	Meaning
0	INSB	An unmasked bit in the instrument status register (INSR) has been set.
1	Reserved	
2	Reserved	
3	Reserved	
4	MAV	The interface output buffer is non-empty
5	ESB	An unmasked bit in the standard event status register (*ESR) has been set.
6	MSS	Master summary bit. Indicates that the instrument is requesting service because an unmasked bit in this register has been set.
7	Reserved	

The serial poll status byte may be queried with the *STB? command. The service request enable register (*SRE) may be used to control when the instrument asserts the request-for-service line on the GPIB bus.

Standard Event Status Register

Bit	Name	Meaning
0	OPC	Operation complete. All previous commands have completed. See command *OPC.
1	Reserved	
2	QYE	Query error occurred.
3	DDE	Device dependent error occurred.
4	EXE	Execution error. A command failed to execute correctly because a parameter was invalid.
5	CME	Command error. The parser detected a syntax error.
6	Reserved	
7	PON	Power on. The unit has been power cycled.

The standard event status register may be queried with the *ESR? command. The standard event status enable register (*ESE) may be used to control the setting of the ESB summary bit in the serial poll status byte.

Instrument Status Register

Bit	Name	Meaning
0	20MHZ_UNLK	The 20 MHz PLL has come unlocked.
1	100MHZ_UNLK	The 100 MHz PLL has come unlocked.
2	19MHZ_UNLK	The 19 MHz PLL has come unlocked.
3	1GHZ_UNLK	The 1 GHz PLL has come unlocked.
4	4GHZ_UNLK	The 4 GHz PLL has come unlocked.
5	NO_TIMEBASE	An installed optional timebase is not oscillating.
6	RB_UNLK	An installed Rubidium timebase is unlocked.
7	Reserved	
8	MOD_OVLD	An internal/external modulation overload was detected.
9	IQ_OVLD	An internal/external IQ modulation overload was detected.
10-15	Reserved	

The instrument status register may be queried with the INSR? command. The instrument status enable register (INSE) may be used to control the setting of the INSB summary bit in the serial poll status byte.

List Mode

The instrument supports a powerful list mode, only available via the remote interface, which enables the user to store a list of instrument states in memory and quickly switch between states by sending GPIB bus triggers or the *TRG command.

WARNING: list mode occupies the same memory space as the internal baseband generator. Therefore, list mode cannot be used with the internal baseband generator. The two modes are mutually exclusive.

List Instrument States

At the heart of the list configuration is the instrument state which should be loaded upon the reception of each valid trigger. The instrument state is downloaded to the unit via the command: LSTP i {, <st>}. The parameter i is the index identifying the list entry to which the instrument state, <st>, should be stored. The instrument state, <st>, consists of an ordered, comma-separated list of 15 values. The order and description of each value is summarized in Table 44.

Note that references to the clock option or the RF doubler do not apply to the SG390 series generators. They are only included to maintain compatibility with the SG380 series generators.

Also listed in the table are related, non-list, commands that also change the given instrument state. For example, frequency is the first parameter. Entering a value here would change the carrier frequency to the given value just as the FREQ command would do.

The parameter for each state is set with a floating point value or integer in the default units as specified by the related commands. For example, entering a 100e6 in the first position would set the frequency to 100 MHz.

Although, all parameters in <st> must be specified, each parameter may be specified as 'N' to leave the parameter unchanged. Thus, to leave all parameters unchanged, set the state as follows:

<All unchanged> = N,N,N,N,N,N,N,N,N,N,N,N,N,N,N

This is the default for all entries when a list is created. To change just one item, simply specify that one item and leave all others unchanged. For example, to only change the BNC output amplitude use the following state:

<BNC ampl: –2 dBm> = N,N,-2.00,N,N,N,N,N,N,N,N,N,N,N,N

Performing scans of frequency or amplitude consists of storing successive instrument list states in which only the frequency is changed, or only the amplitude is changed, respectively. To scan frequency and amplitude simultaneously, simply specify both frequency and amplitude for each state. For example, to change the frequency to 10 MHz and the BNC output to –2 dBm use the following state:

<Freq. and BNC ampl> = 10e6,N,-2.00,N,N,N,N,N,N,N,N,N,N,N,N

If a given setting happens to be invalid when the triggered state occurs, the parameter will be ignored. This might happen, for instance, if one tries to enable pulse modulation with the frequency set to 7 GHz.

Table 44: List State Definitions

Position	Instrument State	Related Commands
1	Frequency	FREQ
2	Phase	PHAS
3	Amplitude of LF (BNC output)	AMPL
4	Offset of LF (BNC output)	OFSL
5	Amplitude of RF (Type N output)	AMPR
6	Front panel display	DISP
7	Enables/Disables Bit 0: Enable modulation Bit 1: Disable LF (BNC output) Bit 2: Disable RF (Type N output) Bit 3: Disable Clock output Bit 4: Disable HF (RF doubler output)	 MODL ENBL ENBR (not applicable) (not applicable)
8	Modulation type	TYPE
9	Modulation function AM/FM/ ΦM Sweep Pulse/Blank IQ	 MFNC SFNC PFNC QFNC
10	Modulation rate AM/FM/ΦM modulation rate Sweep rate Pulse/Blank period	 RATE SRAT PPER, RPER
11	Modulation deviation AM FM ΦM Sweep Pulse/Blank	 ADEP, ANDP FDEV, FNDV PDEV, PNDV SDEV PWID
12	Amplitude of clock output	(not applicable)
13	Offset of clock output	(not applicable)
14	Amplitude of HF (RF doubler output)	(not applicable)
15	Offset of rear DC	(not applicable)

Enables/Disables

The enables/disables setting at position 7 in the state list is different from the others in that multiple commands are aggregated into one value and the polarities of the disables are opposite to that of their corresponding commands. Modulation enable is assigned to bit 0. The output disables are assigned to bits 1 to 4. The enable/disables value is then calculated as the binary weighted sum of all the bits.

For example, to enable modulation and disable the BNC output, we need to set bits 0 and 1. The binary weighted sum is given as $2^0 + 2^1 = 1 + 2 = 3$

Thus, a value of 3 in position 7 would enable the modulation and disable the BNC output.

Modulation List States

Virtually all modulation parameters may be specified as part of a list state, but not simultaneously. In order to compress the size of the list, many parameters share the same position as indicated in Table 19. Thus, in order to untangle which parameters are being specified, the modulation type must be specified. Furthermore, if modulation rate or deviation is specified, then both the modulation type and modulation function must also be specified.

For example, to set AM sine wave modulation depth to 25 %, specify the list state as follows:

<Mod AM: 25%> = N,N,N,N,N,N,N,0,0,N,25.0,N,N,N,N

Similarly, to set FM sine wave modulation deviation to 100 kHz, specify the list state as follows:

<Mod FM: 100 kHz> = N,N,N,N,N,N,N,1,0,N,100e3,N,N,N,N

Specify a frequency sweep of 100 MHz at a 10 Hz rate with a 750 MHz carrier and modulation enabled as follows:

<Sweep: 100 MHz at 10 Hz> = 750e6,N,N,N,N,N,1,3,1,10.0,100e6,N,N,N,N

Specify pulse modulation with a 1 ms period and 10 μs width as follows:

<Mod pulse: 1 ms period, 10 μs width> = N,N,N,N,N,N,N,4,3,1e-3,10e-6,N,N,N,N

Note that although the modulation type and modulation function must usually be specified together, the modulation itself need not necessarily be enabled. Thus, one could configure the modulation in one list entry and enable it in another entry.

Examples

Example 1: Scan frequency from 100 MHz to 1 GHz in 100 MHz steps.

```
LSTC? 10
LSTP 0,100e6,N,N,N,N,N,N,N,N,N,N,N,N,N,N
LSTP 1,200e6,N,N,N,N,N,N,N,N,N,N,N,N,N,N
LSTP 2,300e6,N,N,N,N,N,N,N,N,N,N,N,N,N,N
LSTP 3,400e6,N,N,N,N,N,N,N,N,N,N,N,N,N,N
LSTP 4,500e6,N,N,N,N,N,N,N,N,N,N,N,N,N,N
LSTP 5,600e6,N,N,N,N,N,N,N,N,N,N,N,N,N,N
LSTP 6,700e6,N,N,N,N,N,N,N,N,N,N,N,N,N,N
LSTP 7,800e6,N,N,N,N,N,N,N,N,N,N,N,N,N,N
LSTP 8,900e6,N,N,N,N,N,N,N,N,N,N,N,N,N,N
LSTP 9,1000e6,N,N,N,N,N,N,N,N,N,N,N,N,N,N
LSTE 1
```

Example 2: Scan RF Type N output from 10 dBm to -10 dBm in 5 dBm steps.

```
LSTC? 5
LSTP 0,N,N,N,N,10.0,N,N,N,N,N,N,N,N,N,N
LSTP 1,N,N,N,N,5.0,N,N,N,N,N,N,N,N,N,N
LSTP 2,N,N,N,N,0.0,N,N,N,N,N,N,N,N,N,N
LSTP 3,N,N,N,N,-5.0,N,N,N,N,N,N,N,N,N,N
LSTP 4,N,N,N,N,-10.0,N,N,N,N,N,N,N,N,N,N
LSTE 1
```

Example 3: Configure pulse modulation with 1 ms period and scan the width from 100 µs to 900 µs in 100 µs steps.

```
LSTC? 9
LSTP 0,N,N,N,N,N,N,1,4,3,1e-3,100e-6,N,N,N,N
LSTP 1,N,N,N,N,N,N,N,4,3,N,200e-6,N,N,N,N
LSTP 2,N,N,N,N,N,N,N,4,3,N,300e-6,N,N,N,N
LSTP 3,N,N,N,N,N,N,N,4,3,N,400e-6,N,N,N,N
LSTP 4,N,N,N,N,N,N,N,4,3,N,500e-6,N,N,N,N
LSTP 5,N,N,N,N,N,N,N,4,3,N,600e-6,N,N,N,N
LSTP 6,N,N,N,N,N,N,N,4,3,N,700e-6,N,N,N,N
LSTP 7,N,N,N,N,N,N,N,4,3,N,800e-6,N,N,N,N
LSTP 8,N,N,N,N,N,N,N,4,3,N,900e-6,N,N,N,N
LSTE 1
```

Example 4: Configure AM modulation at1 kHz rate and scan the depth from 25 % to 100 % in 25 % steps.

```
LSTC? 4
LSTP 0,N,N,N,N,N,N,1,0,0,1e3,25,N,N,N,N
LSTP 1,N,N,N,N,N,N,N,0,0,N,50,N,N,N,N
LSTP 2,N,N,N,N,N,N,N,0,0,N,75,N,N,N,N
LSTP 3,N,N,N,N,N,N,N,0,0,N,100,N,N,N,N
LSTE 1
```

Error Codes

The instrument contains an error buffer that may store up to 20 error codes associated with errors encountered during power-on self tests, command parsing, or command execution. The ERR LED will be highlighted when a remote command fails for any reason. The errors in the buffer may be read one by one by executing successive LERR? commands. The user may also view the errors from the front panel by pressing the keys [SHIFT], 'STATUS', sequentially, followed by ADJUST △ until the display reads 'Error Status.' Finally, press SELECT ▷ successively to view the error count and individual errors. The errors are displayed in the order in which they occurred. The ERR LED will go off when all errors have been retrieved.

The meaning of each of the error codes is described below.

Execution Errors

0 No Error

No more errors left in the queue.

10 Illegal Value

A parameter was out of range.

11 Illegal Mode

The action is illegal in the current mode. This might happen, for instance, if the user tries to turn on IQ modulation with the 'MODL 1' command and the current frequency is below 400 MHz.

12 Not Allowed

The requested action is not allowed because the instrument is locked by another interface.

13 Recall Failed

The recall of instrument settings from nonvolatile storage failed. The instrument settings were invalid.

14 No Clock Option

The requested action failed because the rear clock option is not installed.

15 No RF Doubler Option

The requested action failed because the rear RF doubler option is not installed.

16 No IQ Option

The requested action failed because the rear IQ option is not installed.

17 Failed Self Test

This value is returned by the *TST? command when the self test fails.

Query Errors

30 Lost Data

Data in the output buffer was lost. This occurs if the output buffer overflows or if a communications error occurs and data in output buffer is discarded.

32 No Listener

This is a communications error that occurs if the unit is addressed to talk on the GPIB bus, but there are no listeners. The unit discards any pending output.

Device Dependent Errors

40 Failed ROM Check

The ROM checksum failed. The firmware code is likely corrupted.

42 Failed EEPROM Check

The test of EEPROM failed.

43 Failed FPGA Check

The test of the FPGA failed.

44 Failed SRAM Check

The test of the SRAM failed.

45 Failed GPIB Check

The test of GPIB communications failed.

46 Failed LF DDS Check

The test of the LF DDS communications failed.

47 Failed RF DDS Check

The test of the RF DDS communications failed.

48 Failed 20 MHz PLL

The test of the 20 MHz PLL failed.

49 Failed 100 MHz PLL

The test of the 100 MHz PLL failed.

50 Failed 19 MHz PLL

The test of the 19 MHz PLL failed.

51 Failed 1 GHz PLL

The test of the 1 GHz PLL failed.

52 Failed 4 GHz PLL

The test of the top octave PLL failed.

53 Failed DAC

The test of the internal DACs failed.

File System Errors

80 Out of Memory

Not enough memory to store the waveform.

81 File Does Not Exist

File does not exist.

82 File Not Open

Cannot access a file that is not open.

83 File Not Writable

File cannot be written.

84 File Already Exists

Cannot create a file that already exists.

85 File Corrupt

File has been corrupted.

86 End of File

Cannot read passed the end of the file.

87 File Locked

Cannot access a file because it is locked by another user.

Parsing Errors

110 Illegal Command

The command syntax used was illegal. A command is normally a sequence of four letters, or a '*' followed by three letters.

111 Undefined Command

The specified command does not exist.

112 Illegal Query

The specified command does not permit queries

113 Illegal Set

The specified command can only be queried.

114 Null Parameter

The parser detected an empty parameter.

115 Extra Parameters

The parser detected more parameters than allowed by the command.

116 Missing Parameters

The parser detected missing parameters required by the command.

117 Parameter Overflow

The buffer for storing parameter values overflowed. This probably indicates a syntax error.

118 Invalid Floating Point Number

The parser expected a floating point number, but was unable to parse it.

120 Invalid Integer

The parser expected an integer, but was unable to parse it.

121 Integer Overflow

A parsed integer was too large to store correctly.

122 Invalid Hexadecimal

The parser expected hexadecimal characters but was unable to parse them.

126 Syntax Error

The parser detected a syntax error in the command.

127 Illegal Units

The units supplied with the command are not allowed.

128 Missing Units

The units required to execute the command were missing.

Communication Errors

170 Communication Error

A communication error was detected. This is reported if the hardware detects a framing, or parity error in the data stream.

171 Over run

The input buffer of the remote interface overflowed. All data in both the input and output buffers will be flushed.

Other Errors

254 Too Many Errors

The error buffer is full. Subsequent errors have been dropped.

Example Programming Code

The following program can be used as sample code for communicating with the instrument over TCP/IP. The program is written in the C++ language and should compile correctly on a Windows based computer. It could be made to work on other platforms with minor modifications. In order to use the program, you will need to connect the unit to your LAN and configure it with an appropriate IP address. Contact your network administrator for details on how to do this. To identify the unit's current IP address from the front panel, press [SHIFT], [STATUS], then press [△] until the 'tcp ip status' menu appears. Finally press the [◁] [▷] to sequence to the 'ip' address.

Copy the program into a file named "sg_ctrl.cpp". To avoid typing in the program manually, download the electronic version of this manual from the SRS website (www.thinksrs.com). Select the program text and copy/paste it into the text editor of your choice. Compile the program into the executable "sg_ctrl.exe". At the command line type something like the following:

```
sg_ctrl 192.168.0.5
```

where you will replace "192.168.0.5" with the IP address of the unit. You should see the something like the following:

```
Connection Succeeded
Stanford Research Systems,SG394,s/n001013,ver1.00.10A
Closed connection
```

The program connects to the unit at the supplied IP address sets several parameters and then closes. If successful, the frequency should be set to 50 MHz and the amplitudes of Type N and BNC outputs will be set to –10 and –5 dBm, respectively.

```c
/* sg_ctrl.c : Sample program for controlling the SG394 via TCP/IP */
#include "Winsock2.h"
#include <stdio.h>

/* prototypes */
void init_tcpip(void);
int sg_connect(unsigned long ip);
int sg_close(void);
int sg_write(char *str);
int sg_write_bytes(const void *data, unsigned num);
int sg_read(char *buffer, unsigned num);

SOCKET sSG394;                /* SG394 tcpip socket */
unsigned sg_timeout = 6000;   /* Read timeout in milliseconds */

int main(int argc, char * argv[])
{
  char buffer[1024];

  /* Make sure ip address is supplied on the command line */
  if ( argc < 2 ) {
    printf("Usage: sg_ctrl IP_ADDRESS\n");
    exit(1);
  }

  /* Initialize the sockets library */
  init_tcpip();

  /* Connect to the SG394 */
  if ( sg_connect( inet_addr(argv[1]) ) ) {
    printf("Connection Succeeded\n");

    /* Get identification string */
    sg_write("*idn?\n");
    if ( sg_read(buffer,sizeof(buffer)) )
      printf(buffer);
    else
      printf("Timeout\n");
    /* Reset instrument */
    sg_write("*rst\n");
    /* Set frequency to 50 MHz */
    sg_write("freq 50e6\n");
    /* Set amplitude of Type N output to -10 dBm */
    sg_write("ampr -10.0\n");
    /* Set amplitude of BNC output to -5 dBm */
    sg_write("ampl -5.0\n");
    /* Make sure all commands have executed before closing connection */
    sg_write("*opc?\n");
    if ( !sg_read(buffer,sizeof(buffer)) )
      printf("Timeout\n");
    /* Close the connection */
    if (sg_close())
      printf("Closed connection\n");
    else
      printf("Unable to close connection");
  }
  else
    printf("Connection Failed\n");

  return 0;
}
```

```
void init_tcpip(void)
{
  WSADATA wsadata;
  if ( WSAStartup(2, &wsadata) != 0 ) {
    printf("Unable to load windows socket library\n");
    exit(1);
  }
}

int sg_connect(unsigned long ip)
{
  /* Connect to the SG394 */
  struct sockaddr_in intrAddr;
  int status;

  sSG394 = socket(AF_INET,SOCK_STREAM,0);
  if ( sSG394 == INVALID_SOCKET )
    return 0;

  /* Bind to a local port */
  memset(&intrAddr,0,sizeof(intrAddr));
  intrAddr.sin_family = AF_INET;
  intrAddr.sin_port = htons(0);
  intrAddr.sin_addr.S_un.S_addr = htonl(INADDR_ANY);
  if ( SOCKET_ERROR == bind(sSG394,(const struct sockaddr *)&intrAddr,sizeof(intrAddr)) ) {
    closesocket(sSG394);
    sSG394 = INVALID_SOCKET;
    return 0;
  }

  /* Setup address for the connection to sg on port 5025 */
  memset(&intrAddr,0,sizeof(intrAddr));
  intrAddr.sin_family = AF_INET;
  intrAddr.sin_port = htons(5025);
  intrAddr.sin_addr.S_un.S_addr = ip;
  status = connect(sSG394,(const struct sockaddr *)&intrAddr,sizeof(intrAddr));
  if ( status ) {
    closesocket(sSG394);
    sSG394 = INVALID_SOCKET;
    return 0;
  }
  return 1;
}

int sg_close(void)
{
  if ( closesocket(sSG394) != SOCKET_ERROR )
    return 1;
  else
    return 0;
}

int sg_write(char *str)
{
  /* Write string to connection */
  int result;

  result = send(sSG394,str,(int)strlen(str),0);
  if ( SOCKET_ERROR == result )
    result = 0;
  return result;
}
```

```
int sg_write_bytes(const void *data, unsigned num)
{
  /* Write string to connection */
  int result;

  result = send(sSG394,(const char *)data,(int)num,0);
  if ( SOCKET_ERROR == result )
    result = 0;
  return result;
}

int sg_read(char *buffer, unsigned num)
{
  /* Read up to num bytes from connection */
  int count;
  fd_set setRead, setWrite, setExcept;
  TIMEVAL tm;

  /* Use select() so we can timeout gracefully */
  tm.tv_sec = sg_timeout/1000;
  tm.tv_usec = (sg_timeout % 1000) * 1000;

  FD_ZERO(&setRead);
  FD_ZERO(&setWrite);
  FD_ZERO(&setExcept);
  FD_SET(sSG394,&setRead);
  count = select(0,&setRead,&setWrite,&setExcept,&tm);
  if ( count == SOCKET_ERROR ) {
    printf("select failed: connection aborted\n");
    closesocket(sSG394);
    exit(1);
  }
  count = 0;
  if ( FD_ISSET(sSG394,&setRead) ) {
    /* We've received something */
    count = (int)recv(sSG394,buffer,num-1,0);
    if ( SOCKET_ERROR == count ) {
      printf("Receive failed: connection aborted\n");
      closesocket(sSG394);
      exit(1);
    }
    else if (count ) {
      buffer[count] = '\0';
    }
    else {
      printf("Connection closed by remote host\n");
      closesocket(sSG394);
      exit(1);
    }
  }
  return count;
}
```

SG390 Series Operation Verification

Overview

The operation of a SG390 series RF signal generator may be evaluated by running a series of tests designed to measure the accuracy of its inputs and outputs and comparing the results with their associated specifications. While the verification tests presented here are not as extensive as the tests performed at the factory, one can nevertheless have confidence that a unit that passes these tests is functioning properly and within specification.

The verification tests can be divided into three broad categories: output driver tests, frequency synthesis tests, and timebase calibration tests. The output driver tests are designed to test the integrity and accuracy of the front panel outputs by measuring the output power of the BNC and Type N outputs. The frequency synthesis tests verify the overall frequency generation at various points in the spectrum from DC to 6 GHz. Lastly, the timebase calibration tests evaluate the accuracy and stability of the installed timebase.

Please allow the instrument under test to warm up for 1 hour before testing it to a specification.

Equipment Required

In addition to the SG390 series RF signal generator under test, the following equipment will be required to carry out the performance tests:

- Agilent U2004A power meter: 9 kHz to 6 GHz
- Agilent E4440A PSA Spectrum Analyzer
- Agilent DSO-X-2014A oscilloscope
- Agilent 34410A DVM
- SRS DS345 function generator
- SRS FS725 rubidium frequency standard
- SRS SR620 time interval counter

Equivalent equipment may be substituted as desired as long as they have similar or superior specifications. Standard BNC and shielded SMA and Type N cables will be required to connect the test equipment to the SG390 series generators. Additionally accessories required include 50 Ω terminators and various adapters.

SG390 Series Self Test

The SG390 series RF signal generators include a self test that checks the functional operation of many important internal components. If any of the tests fail, the unit will briefly display “Failed” after the test.

The SG390 series self test may be executed from the front panel by performing the following steps:

1. Press the keys [SHIFT], [0], and [Hz] to reset the instrument to default settings.
2. Press the keys [SHIFT], [2], ADJUST [△], and [Hz] to run the self test.

The self test may also be run by sending the commands ***RST;*TST?** over a remote interface. If the unit passes it will return 0 over the remote interface. If it fails, it will return 17. Further information about the specific tests that failed may be accessed from the front panel by pressing the keys [SHIFT], [2] and pressing ADJUST [△] until the display reads “Error Status.” Press SELECT [▷] successively to view each error code. The error codes are detailed in the Remote Programming section of the operation manual.

Output Power Tests

The output power tests are intended to test the integrity of the SG390 series output blocks. They test the output power of the front panel BNC and Type N outputs at various frequencies.

BNC Output Power Test

The BNC output power test requires the setup shown in Figure 69. The power meter plus adapter should be connected directly to the BNC output with no intervening cable.

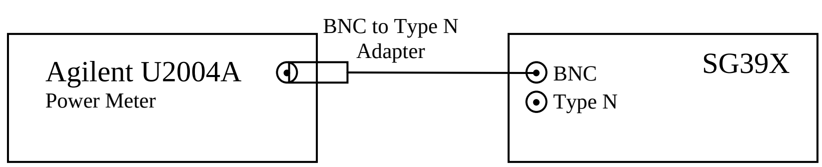


Figure 69: BNC output power test setup

To verify the integrity of the BNC output, perform the following procedures:

1. Before attaching the power meter to the SG390 series unit under test, calibrate and zero the power meter.
2. Attach the power meter to the SG390 series unit under test.
3. Set the calibration frequency for the power meter to the test frequency given in Table 45.
4. On the SG390 series generator, press the keys [SHIFT], [0], and [Hz] to reset the instrument to default settings.

5. Press [FREQ] to select frequency. Then enter the test frequency given in Table 45.
6. Press [AMPL] until the display shows “bnc”. Then enter the power setting given in Table 45.
7. Record the power reported by the power meter. Verify that it is within the stated limits.
8. Repeat step 3 followed by steps 5 through 7 for each frequency and power setting in Table 45.

Table 45: Power level requirements for the BNC output

Frequency	Power Setting (dBm)	Measured Power (dBm)	Limits (dB)
10 MHz	10.0		±2
	5.0		±2
	0.0		±2
	-5.0		±2
	-10.0		±2
50 MHz	10.0		±2
	5.0		±2
	0.0		±2
	-5.0		±2
	-10.0		±2

Type N Output Power Test

The Type N output power test requires the setup shown in Figure 70. The power meter should be attached directly to the Type N output of the SG390 series unit under test with no intervening cable

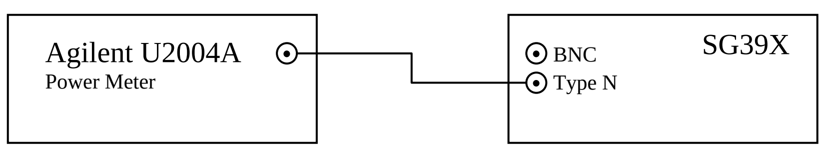


Figure 70: Type N output power test setup

To verify the integrity of the Type N output perform the following procedures:

1. Before attaching the power meter to the SG390 series unit under test, calibrate and zero the power meter.
2. Attach the power meter to the SG390 series unit under test.
3. Set the calibration frequency for the power meter to the test frequency given in Table 46.
4. On the SG390 series generator, press the keys [SHIFT], [0], and [Hz] to reset the instrument to default settings.
5. Press [FREQ] to select frequency. Then enter the test frequency given in Table 46.

6. Press [AMPL] until the display shows “ntype”. Then enter the power setting given in Table 46.
7. Record the power reported by the power meter. Verify that it is within the stated limits.
8. Repeat step 3, followed by steps 5 through 7 for each frequency and power setting in Table 46.

Table 46: Power level requirements for the Type N output

Frequency	Power Setting (dBm)	Measured Power (dBm)	Limits (dB)
50 MHz	10.0		±2
	5.0		±2
	0.0		±2
	-5.0		±2
	-10.0		±2
100 MHz	10.0		±2
	5.0		±2
	0.0		±2
	-5.0		±2
	-10.0		±2
250 MHz	10.0		±2
	5.0		±2
	0.0		±2
	-5.0		±2
	-10.0		±2
500 MHz	10.0		±2
	5.0		±2
	0.0		±2
	-5.0		±2
	-10.0		±2
1000 MHz	10.0		±2
	5.0		±2
	0.0		±2
	-5.0		±2
	-10.0		±2
2000 MHz	10.0		±2
	5.0		±2
	0.0		±2
	-5.0		±2
	-10.0		±2
4000 MHz	10.0		±2
	5.0		±2
	0.0		±2
	-5.0		±2
	-10.0		±2
6000 MHz	10.0		±2
	5.0		±2
	0.0		±2
	-5.0		±2
	-10.0		±2

The measurements at 4000 MHz only apply to the SG394 and SG396. The measurements at 6000 MHz only apply to the SG396.

Frequency Synthesis Tests

Basic functionality of the SG390 series generators is verified by testing the generation of several specific frequencies from DC to 6 GHz.

Frequency Generation Tests

Frequency generation tests verify that basic frequency synthesis of the device under test is operating correctly. This is accomplished by measuring the output frequency of the SG390 series generator at several specific frequencies from DC to 6 GHz. The specific frequencies selected in the test guarantee that all crystals within the device under test are functioning properly and that all phase locked loops are locked and stable. The Agilent E4440A PSA spectrum analyzer is used to verify frequency synthesis. This test requires the setup shown in Figure 71.

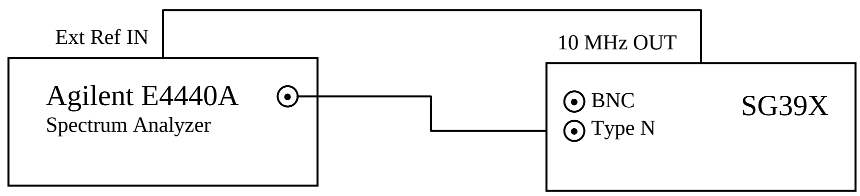


Figure 71: Setup for frequency generation tests.

To verify the frequency generation of the device under test perform the following procedures:

1. Connect the equipment as shown in Figure 71
2. Verify that the spectrum analyzer is locked to the 10 MHz external reference frequency.
3. Align the spectrum analyzer by pressing the keys [System], [Alignment], [Align All Now].
4. On the SG390 series generator, press the keys [SHIFT], [0], and [Hz] to reset the instrument to default settings.
5. Press [AMPL] until the display shows “ntype”. Then press [0], [dBm] to set the amplitude to 0 dBm.
6. Press [FREQ] to select frequency. Then enter the test frequency given in Table 47.
7. Verify that the measured frequency is within the limits given in Table 47.
8. Repeat steps 6 and 7 for all the frequencies given in Table 47

Note that frequencies above 2025 MHz do not apply to the SG392. Similarly, frequencies above 4050 MHz do not apply to the SG394. All test frequencies apply to the SG396.

Table 47: Test frequencies for frequency synthesis

Test Freq. (MHz)	Measured Freq. (MHz)	Limit (Hz)
50		±2
99		±2
177		±2
250		±2
333		±2
498		±2
723		±2
1000		±2
1522		±2
2013		±2
2845		±2
3350		±2
3999		±2
4650		±2
5319		±2
6000		±2

Modulation Output Test

This is test verifies the operation of the modulation engine and the modulation output. It does not test to any specifications. This test requires the setup shown in Figure 72

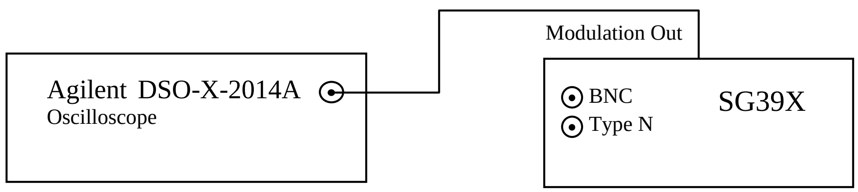


Figure 72: Setup for modulation output test.

To verify the operation of the modulation output, use the following procedure:

1. Connect the equipment as shown in Figure 72.
2. Set the scope to trigger on Ch 1, rising edge
3. Set the vertical scale to 500 mV/div
4. Set the timebase to 500 us/div
5. On the SG390 series generator, press the keys [SHIFT], [0], and [Hz] to reset the instrument to default settings.
6. Press [MOD FCN] and then press ADJUST [▽] two times. The display should read “func triangle.”
7. Press [ON/OFF] to turn the modulation on.

The waveform on the scope should look similar to that shown in Figure 73. It should be a 1 kHz triangle wave centered about 0 V with a peak to peak deviation of 2 V. Verify that the waveform has no discontinuities.

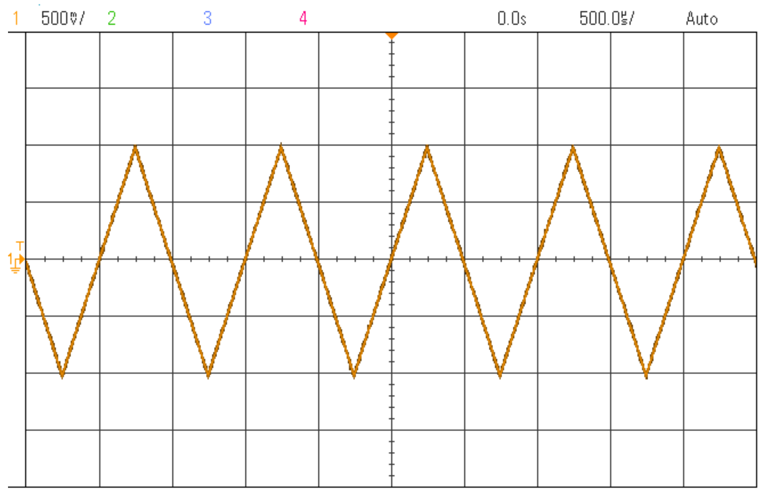


Figure 73: Modulation output waveform.

Modulation Input Test

This is test verifies the operation of the modulation engine and modulation input. It does not test to any specifications. This test requires the setup shown in Figure 74

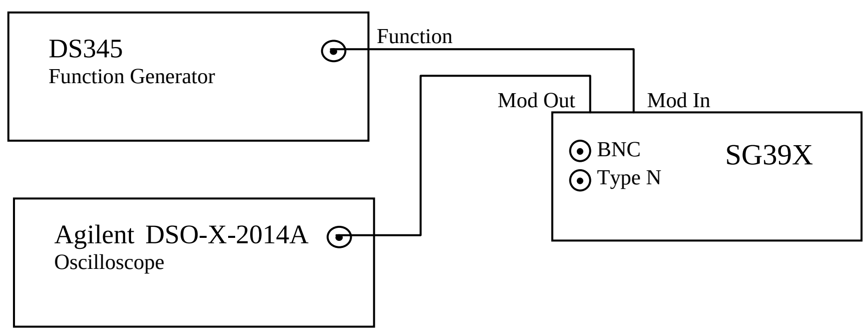


Figure 74: Setup for modulation input test.

To verify the operation of the modulation input, use the following procedure:

1. Connect the equipment as shown in Figure 74.
2. Set the scope to trigger on Ch 1, rising edge
3. Set the vertical scale to 500 mV/div
4. Set the timebase to 500 us/div
5. Reset the DS345 to default settings by pressing [SHIFT], [RCL]
6. Set the DS345 for triangle waves by pressing FUNCTION [▽] twice.
7. Set the DS345 for a 1 Vpp output by pressing the keys [AMPL], [1], [Vpp].
8. On the SG390 series generator, press the keys [SHIFT], [0], and [Hz] to reset the instrument to default settings.

9. Select external modulation by pressing [MOD FCN] and then pressing ADJUST [▽] until the "EXT" LED is highlighted. The display should read "rear input ac dc"

10. Press [ON/OFF] to turn the modulation on.

The waveform on the scope should look similar to that shown in Figure 75. It should be a 1 kHz triangle wave centered about 0 V with a peak to peak deviation of 2 V. Verify that the waveform has no discontinuities.

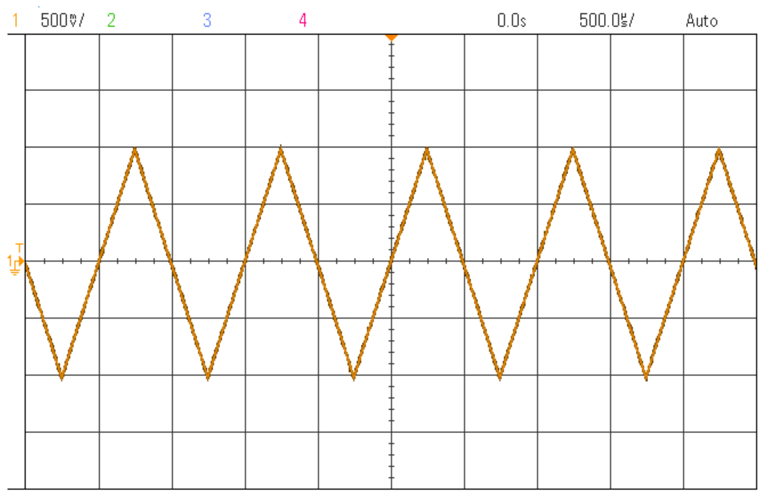


Figure 75: Modulation input test waveform.

IQ Modulation Test

This test verifies the operation of the IQ modulator. This test requires the setup shown in **Error! Reference source not found.**

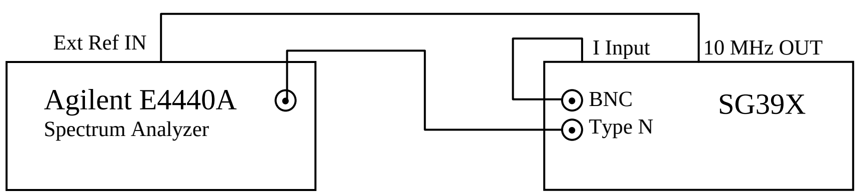


Figure 76: Option 3 IQ modulator test.

To verify the operation of the IQ modulator use the following procedure:

1. Connect the equipment as shown in **Error! Reference source not found.**
2. Verify that the spectrum analyzer is locked to the 10 MHz external reference frequency.
3. Align the spectrum analyzer by pressing the keys [System], [Alignment], [Align All Now].
4. On the SG390 series generator, press the keys [SHIFT], [0], and [Hz] to reset the instrument to default settings.
5. Press [FREQ], [1], [GHz] to set the frequency to 1 GHz

6. Press [MOD TYPE] and then press ADJUST [▽] until the ΦM/PSK LED is highlighted. Press SELECT [▷]. The display should read “vector PM func.”
7. Press [MOD FCN] and then press ADJUST [▽] until the EXT LED is highlighted. The display should read “Fn rear iq input.”
8. Press [DC OFFS] successively until the display reads “bnc”
9. Press [0], [.], [5], [Vpp] to set the DC offset to 0.5 V.
10. Measure the amplitude of the 1 GHz signal on the Agilent spectrum analyzer.
11. Press [ON/OFF] to enable external IQ modulation.
12. Measure the amplitude of the 1 GHz signal on the Agilent spectrum analyzer.
13. Disconnect the BNC cable from the rear panel I input.
14. Measure the amplitude of the 1 GHz signal on the Agilent spectrum analyzer.

The difference between the values recorded in step 10 and step 12 should be less than 1 dB. The difference between the values recorded in step 12 and step 14 should be greater than 40 dB.

Timebase Calibration

The accuracy of the internal timebase may be tested against a house reference if it is known that the house reference has a superior stability and accuracy than the timebase installed in the SG390 series generator. Use the setup shown in Figure 77 to test the accuracy of the timebase.

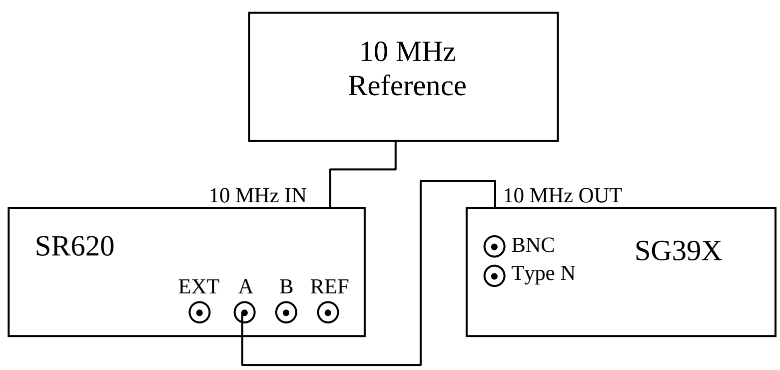


Figure 77: Setup for timebase calibration

The accuracy and stability of the SG390 series timebase depends on the type of timebase installed. An optional timebase, if installed, can be identified on the rear panel of SG390 series generator under the serial number with the label “Rubidium Timebase”

If the standard OCXO timebase is installed, an FS725 Rb frequency standard may be used as the 10 MHz reference. If a rubidium timebase is installed, a cesium based reference will be required as a reference.

SR620 Configuration

Use the following procedure to set up the SR620:

1. With the power off hold down the [CLR] button in the DISPLAY section and turn the power on. This resets the SR620 to default settings.
2. Press [SEL] in the CONFIG section until “CAL” is flashing
3. Press [SET] in the CONFIG section until “cloc Source” is displayed
4. Press SCALE[△] in the SCOPE AND CHART section until “cloc Source rear” is displayed
5. Press MODE [▽] button until the selected mode is FREQ.
6. Press [SEL] in the CONFIG section until “OUT” is flashing
7. Press [SET] in the CONFIG section until “Gate Scale” is displayed
8. Press SCALE[△] in the SCOPE AND CHART section until 100 is displayed.
9. Press the DISPLAY [△] to return to the normal display
10. Press the GATE/ARM [△] button once to set the gate to 10 s
11. If a rubidium timebase is installed in the SG390 series generator, press the GATE/ARM [△] button once more to set the gate to 100 s
12. Press the SAMPLE SIZE [▽] button three times to set the sample size to 1.
13. Turn the trigger level knob above the channel A input counter clockwise until AUTO is highlighted.
14. Press the channel A [INPUT] button once to switch to 50 Ω termination.

Timebase Calibration Test

It is critical that the timebase be fully warmed up before measurements are taken. Allow at least 1 hour of warm-up for installed timebase to stabilize.

Record the timebase frequency reported by the SR620. Compare it to the stated one-year accuracy shown in Table 48 for the installed timebase.

Table 48: Timebase calibration test

Timebase	Freq. (MHz)	Measured Freq. (MHz)	Limit (Hz)
Standard	10		±0.5
Opt 4: Rubidium	10		±0.01

Calibration

The SG390 series internal timebase may be calibrated from the front panel using the measurements taken above. The process is iterative. Use the following procedure to calibrate the internal timebase:

1. Press [SHIFT], [+/–] to activate the CAL secondary function. Then press Press the SELECT [▷] until the display shows "tcal."
2. Press the ADJUST [△] and [▽] keys to adjust the timebase frequency up or down respectively.
3. Measure the new frequency with the SR620.
4. Repeat steps 2 and 3 until the desired frequency accuracy is achieved.

Conclusions

The tests described in this document are designed to test the basic functionality of the unit. They are not intended to be a substitute for the complete performance test which is performed at the factory. Nevertheless, one can have reasonable confidence that instruments that pass the tests described in this document are operating correctly. As always, if an instrument fails to pass a test, verify that the setup has been duplicated correctly, and that the individual procedures have been followed as specified. Instruments that have failed to meet specifications may be returned to SRS for repair.

Circuit Description

Overview

There are three RF Signal Generators in the SG390 Series: The SG392 (DC to 2.025 GHz), the SG394 (DC to 4.050 GHz) and the SG396 (DC to 6.075 GHz).

Each signal generator has extensive modulation capabilities including analog (AM, FM, ΦM, Sweeps, Pulse) and vector IQ modulation. The units' low phase noise (-116 dBc/Hz at 20 kHz offset at 1 GHz) and high resolution (1 μHz at all frequencies) are provided by a unique synthesis technique that allows essentially infinite frequency resolution together with a high phase comparison frequency without the noise or spurs associated with conventional fractional-N synthesis.

The Sig Gens have a versatile dual baseband generator and high bandwidth, rear panel I/Q modulation inputs.

The standard timebase is an ovenized, 3^{rd} overtone, SC-cut oscillator. Option 4 improves the timebase accuracy by adding a rubidium oscillator.

The three models (SG392, SG394 and SG396) share a common design approach. All units use the same power supply and motherboard (which includes timebase and frequency references, DDS synthesizers, VCXO filters, modulation generator, and computer interfaces).

The RF Block for the SG392 and SG394 is identical, using a 1900 MHz to 4100 MHz VCO and digital dividers to synthesize RF frequencies. The top octave is not used (or calibrated) in the SG392, whose maximum frequency is 2.025 GHz.

The RF Block for the SG396 is different from that used in the SG392 and SG394. The VCO in the SG396 covers from 3 GHz to 6 GHz, and the output amplifier uses a pHEMT gain block instead of the InGaP gain block which is used in the SG392 and SG394.

For brevity, the circuit description which follows will refer to the SG394. Differences between the units will be detailed as required.

Block Diagram

(Schematic 1: Block Diagram)

Important sections of the instrument, and the interconnections between them, are illustrated in the block diagram. We will follow the RF signal path first, and then we will discuss the various support functions.

The RF path starts in the upper left corner with the Timebase and ends in the lower right corner with the Output Amplifiers and Attenuators. The timebase consists of a 20 MHz VCXO that is phase locked to an internal OCXO, to an internal rubidium timebase (Option 4), or to an external 10 MHz reference. A 100 MHz VCXO is phase locked to the 20 MHz timebase. The 100 MHz is divided by four to provide 25 MHz to the CPU and FPGA. The 100 MHz is also the sample clock for a 48-bit DDS (here after referred to as the LF DDS). The frequency resolution of the LF DDS is extended to 64 bits via the FSK pin of the LF DDS. The output frequency of the instrument is proportional to the frequency output of this LF DDS and so this establishes the instrument’s frequency resolution.

The output of the LF DDS cannot serve directly as the reference for the RF synthesizer because spurs on the LF DDS output would appear on the RF output, increased in magnitude by 6 dB per octave between the LF DDS output and the instrument’s RF output. Hence, one of three VCXOs is used to filter the LF DDS output to remove the spurs. Two of the VCXOs can be tuned by ±100 ppm (around 19.5541 MHz or 19.6617 MHz), while the third VCXO can be tuned by ±10 ppm around 19.607843 MHz (collectively referred to hereafter as 19+ MHz VCXO). These frequencies were chosen to maximize the phase comparison frequency in the RF synthesizer’s PLL, as well as optimizing performance at canonical frequencies. The LF DDS is programmed to operate in one of these three ranges and the corresponding VCXO is phase locked to the LF DDS. The output of the phase locked VCXO, whose frequency can now be set with 64 bits of resolution, becomes the timebase for the RF synthesizer.

The selected 19+ MHz VCXO is multiplied up by ×51 to a frequency near 1 GHz by the PLL synthesizer in the RF Reference / Baseband DDS section of the block diagram. The 1 GHz output serves as the sample clock to a 32-bit DDS (hereafter referred to as the RFDDS). The output of the RFDDS becomes the reference frequency for the RF synthesizer. The RFDDS is programmed to divide by an integer when it is used as a reference for an unmodulated RF output. Dividing by an integer eliminates DDS spurs, as the DDS repeats the exact same sequence for every cycle of its divided output and so “spurs” collect together as harmonics which do not cause clock jitter or spurious frequency outputs. When generating frequency or phase modulated outputs the RFDDS provides agile modulation of the RF reference frequency via the 16-bit words from the FPGA modulation processor, which are updated at 125 MHz.

The output of the 1 GHz, 32-bit, RFDDS is filtered and passed differentially to the RF synthesizer in the RF Block to serve as the PLL frequency reference, f_{ref} . A wideband VCO (1900-4100 MHz for the SG392 and SG394, or 3 GHz to 6 GHz for the SG396) is divided by N and phase locked to the reference divided by R, to produce and output a frequency of $f_{ref} \times N / R$. The output of this synthesizer clocks binary dividers to provide square wave outputs in the 5 octaves below the RF VCO frequency. The square waves are low-pass filtered to provide sine wave outputs over the same frequency range. An RF multiplexer selects one of the sine waves, or the original reference sine wave (in the case that the RF output is less than 62.5 MHz (less than 93.75 MHz for the SG396), as the source to the RF output stages.

The selected RF sine wave is passed to the RF Output Amplifiers and Attenuators block. An I/Q modulator is inserted into the signal path when I/Q modulation is being used, otherwise the RF output is passed directly to a series of RF attenuators and amplifiers which provide an output amplitude range from –107 dBm to +16.5 dBm. A voltage variable attenuator is used to provide amplitude modulation. The amplified and attenuated RF sine wave, in the frequency range of 950 kHz to 2, 4 or 6 GHz, is output via the front panel Type N connector.

There is another signal path for output signals between dc and 62.5 MHz. The 32-bit RFDDS on the mother board provides signals in this range directly. The differential signals are passed to the output block and can be amplified or attenuated to a range from $1mV_{rms}$ to $1V_{rms}$ and offset with a dc voltage. The amplified and offset output is passed out the front panel BNC connector via 50 Ω.

There are several modulation paths. As previously described, frequency and phase modulation is provided by the FPGA via the RFDDS's parallel port. The source for the modulation waveform can be a table in the FPGA, data stored in a larger memory external to the FPGA, or up-sampled and digitally filtered data streaming from an ADC which digitizes the rear panel modulation input. An analog copy of the modulation waveform is output via a rear panel BNC.

Analog signals to provide I/Q modulation can originate from a table in the FPGA, or data stored in a larger memory external to the FPGA, up-sampled to 125 MHz, digitally filtered, and output via dual 14-bit DACs. I/Q modulation can also be provided directly via rear panel BNC inputs (Option 3). Copies of the I&Q modulation waveforms can be output via rear panel BNCs (Option 3).

Amplitude modulation can originate from a table in the FPGA, data stored in a larger memory external to the FPGA, or up-sampled data streaming from an ADC which digitizes the rear panel modulation input. RF outputs above 62.5 MHz are amplitude modulated via a voltage variable attenuator in the RF output stages. Outputs below 62.5 MHz are amplitude modulated via the 16-bit parallel port on the RFDDS. An analog copy of the modulation waveform is output via a rear panel BNC.

A Coldfire™ microcontroller is used to control all aspects of the instrument's operation and to interface to external computers via the Ethernet, GPIB or RS-232. The microcontroller also responds to front panel key presses and updates front panel displays.

The front panel display is fully static (there is one latched bit per display segment or indicator lamp.) This approach eliminates the possibility of a display refresh spur in the RF output. The front panel display is written to and read from serially when a change is made or a key is pressed.

The system power supply is enclosed in a separate enclosure within the instrument for safety and shielding. A universal input power supply converts the line voltage to +24 V_{DC} which is always present to provide power to the OCXO or optional rubidium timebase. An inverter operates to provide ±15, ±5, and +3.3 V when the unit is switched "on" to power the rest of the instrument.

Detailed Circuit Description

Several sub-assemblies will be described:

1. The front panel display
2. The front panel display EMI filter
3. The mother board
4. The RF synthesizer
5. The RF output amplifiers and attenuators
6. The power supply
7. I/Q modulation inputs & outputs
8. Option 4 (Rubidium Timebase)

Front-Panel Display

(Schematic 2: Front Panel Display)

The front panel consists of 16 seven-segment displays, 47 LED lamps, and 33 key conductive rubber keypads. The front panel display is fully static in that there is one latched bit for each LED segment or lamp. Data is written to the display serially via the SPI (Serial Peripheral Interface Bus). When a key is pressed, the input to the corresponding latch is pulled high, and a KEYPRESS interrupt is sent to the CPU. Key press data is latched when the CPU responds with a –CS_FRONT. As data is being written to the display, latched key press data is also read back over the SPI.

The lamp currents (which set brightness) are equal to the +3.3 V supply, minus the ~2 V LED voltage, divided by resistance of the current limiting network (100 Ω). The LED display segment current (which sets segment brightness) is equal to +3.3 V supply, minus the ~1.5 V LED voltage, minus the 0.7 V base-emitter voltage of Q1A (for example), divided by resistance of the current limiting network (680 Ω). The intensity of a digit can be increased by turning on the other transistor in the pair (Q1B, for example) by setting Q7 of U43 low and asserting –INTENSIFY, which will cause the voltage on the common anode of U16 to increase by about 0.6 V.

Front-Panel Display EMI Filter

(Schematic 3: Display EMI Filter)

The Front panel Display is shielded from the main box via a metal panel. The SPI interface and power connections are filtered by a separate PCB. These help to eliminate EMI and reduce the display interference in the main system's sensitive electronics.

Motherboard

The motherboard is the large PCB nearest to and approximately the same size as the bottom cover of the instrument. There are eight pages of schematics for the motherboard. Circuits include 10 MHz & 20 MHz timebases, three 19+ MHz VCXOs, Coldfire CPU with Ethernet, GPIB, and RS-232 interfaces, FPGA modulation processor, modulation DACs and external modulation ADC, 1 GHz VCO, an RF reference DDS, and interfaces to the RF Block and the rear panel options.

Timebases

(Schematic 4: Mother Board 1, Frequency Refs)

The timebase reference is a 20 MHz VCXO consisting of the 3rd overtone crystal, Y100, and the Colpitts oscillator, Q100. The crystal is designed to operate with a 20 pF load which is the series combination of C110, the tank L103/C111, and the varactor D100. To provide gain, both C110 and the parallel combination of L103 & C111 must have a capacitive reactance. The L103/C111 tank has an inductive reactance below 8.9 MHz which prevents the oscillator from operating at the fundamental frequency of the crystal. The crystal is operated just above its series resonance, and so has an inductive reactance that resonates with the load capacitance. The operating frequency is controlled by the dc voltage applied to the varactor.

The oscillator's circulating current is cascoded into the emitter of Q101 through to the collector, which is held at dc ground by L105 and amplitude limited by the dual Schottky, U105. The output is amplified and buffered by the low noise amplifier, U107, which provides a (nearly) square wave output with amplitude of about 2.4 Vpp at 20 MHz. This signal is ac coupled and converted to a 3.3 V CMOS level square wave by U114, which is powered by a low noise source, U112.

The 20 MHz square wave can be phase locked to an external timebase reference or to an internal OCXO or optional rubidium oscillator by the PLL synthesizer, U106. The 10 MHz RF input to the PLL synthesizer is selected by the multiplexer U109. Another multiplexer, U103, improves isolation between the internal OCXO or rubidium reference and the external timebase reference.

The presence of an internal reference is detected by the diodes U100 and the corresponding peak detection circuit. The presence of an external reference is detected by the diodes U104 and the corresponding peak detection circuit. The CPU operates the multiplexers to select the external reference whenever it is available, the internal OCXO or rubidium next, or a fixed programming voltage to adjust the 20 MHz VCXO as a last resort.

The PLL synthesizer's charge pump output is conditioned by the loop filter U110B. The loop filter has a bandwidth of about 140 Hz. The multiplexer U108 selects between the charge pump output (when the PLL is active) or a fixed programming voltage, CAL_VCO (when no better reference is available). A lock detect signal is provided to the CPU.

The 20 MHz is divided by two by U115, which drives transformer T100 differentially. The output of the transformer is low pass filtered (with a notch at 30 MHz) to provide the 10 MHz sine wave timebase output on a rear panel BNC.

A 100 MHz VCXO, U119, is phase locked to the 20 MHz reference by U116, a CMOS PLL frequency synthesizer. The differential outputs from the VCXO are used to clock a 48-bit DDS, and converted to CMOS logic levels and divided by 4 to generate 25 MHz clocks for the CPU and FPGA sections.

LF DDS and 19 MHz Reference

(Schematic 5: Mother Board 2, 19 MHz Ref)

The singular purpose of this page of schematics is to produce a low noise "19MHZ_REF" square wave which serves as the reference frequency for the rest of the RF synthesizer chain. A DDS (hereafter referred to as the LF DDS) is used to provide a frequency reference of 19 MHz and a resolution of $1:10^{18}$. Spurs and noise outside of the PLL loop bandwidth are rejected from the DDS output by phase locking a narrowband VCXO to the LF DDS. Spurs at all frequencies are reduced by applying a PRBS (pseudo-random binary sequence) to the FSK (frequency-shift key) input of the LF DDS with a repetition rate of about 98 kHz.

There are three nearly identical VCXOs. Each uses a crystal resonator in a Colpitts oscillator. The middle VCXO (19.607843 MHz) uses a 3rd overtone crystal and so has less phase noise and a narrower tuning range than the other VCXOs. The configuration of the middle VCXO is identical to the 20 MHz timebase described above. The circulating oscillator current is cascoded into the emitter of Q204. The collector load (L204 and back-to-back Schottky diodes U204) shape the signal current into a nearly square wave with no dc offset.

One of the three VCXOs is selected to be phase locked to the LF DDS. The selected VCXO has its output amplifier (U209, U210 or U211) enabled. An output multiplexer (U206, U207 or U208) connects the selected VCXO output to the input of U213, which shapes the selected signal into a CMOS level square wave.

The 100 MHz timebase serves as the clock to a LF DDS (U215) which is programmed to generate frequencies over three ranges: 19.5541 MHz$\pm$100ppm, 19.607843 MHz $\pm$10 ppm and 19.6617 MHz $\pm$100 ppm. The frequency resolution of the 48-bit LF DDS is extended to 64-bits by toggling between two frequency tuning words with a duty cycle that has 16 bits of resolution. The differential output of the LF DDS is transformer coupled to a low pass filter (L217-222 and C252-254) that has a cutoff frequency of 24 MHz.

Spurs and broadband noise are rejected from the output of the LF DDS by phase locking one of three VCXOs to the LF DDS output. The selected VCXO is phase locked by a CMOS PLL synthesizer, U217. One of two loop filters is used: U216A, a loop filter with 400 Hz bandwidth, is used when the selected VCXO is one of the fundamental mode oscillators. U216B, a loop filter with 200 Hz bandwidth, is used when the 3rd overtone oscillator is selected.

Microcontroller and Interface

(Schematic 6: Mother Board 3, CPU)

A Coldfire™ MCF52235 microcontroller is used to control the instrument and to interface to external computers via Ethernet, GPIB or RS-232. The microcontroller uses a 32-bit data path, has 256k of program flash ROM, 32k of RAM, an octal 12-bit ADC, and operates at 60 MHz from a 25 MHz clock input.

The microcontroller's ADCs are used to detect various PLL lock states, detect 10 MHz references, measure the control voltages applied to various VCOs, sense RF block temperature, measure the detected RF output, and measure miscellaneous systems voltages.

One of the microcontroller's UARTs is translated to RS-232 levels by U311 and made available on the rear panel for control by remote computers. The microcontroller's Ethernet controller is connected directly to a RJ-45 connector, U302, which is accessible on the rear panel to connect the instrument to a local area network. An 8-bit bidirectional port is used to interface the microcontroller to a GPIB controller, U316, whose connector is also on the instrument's rear panel.

The microcontroller's SPI (serial peripheral interface bus) is expanded to 16 ports by the decoders U308 and U309. The eight devices which are selected by U309 (PLL synthesizers, RF and Option control) are designated as "quiet" SPI devices. The SPI data and clock signals are only presented to these devices when one in the group is being addressed. Doing so reduces crosstalk disturbances which can add spurs to RF outputs. The AND gates in U312 gate "off" the QSCK and QMOSI signals unless the U309 decoder is enabled.

SPI devices include:

0) Idle, 1) spare, 2) FPGA modulation processor, 3) 19 MHz DDS, 4) RF DDS, 5) cal ROM flash, 6) front panel display, 7) miscellaneous control bits, 8) 20 MHz PLL, 9) 100 MHz PLL, 10) 19 MHz PLL, 11) 1 GHz PLL, 12) 4 GHz PLL, 13) RF block control, 14) Option 1&2 control, 15) system DAC.

Modulation Processor

(Schematic 7: Mother Board 4, Modulation Processor)

A Xilinx XC3S400A in a 320-pin BGA is used as a modulation processor in the SG394. The FPGA is attached to two large memories via a 16-bit data bus. The E28F320J3D75A, U402, is a Numonyx 32 MBit flash memory which is used to store FPGA configurations and user arbitrary waveforms. The CY62167DV30, U400, is a Cypress 16 MBit, 55 ns static RAM used to store and play modulation waveforms.

Several FPGA configurations are stored in the flash memory. Each configuration allows the FPGA to perform a variety of modulation tasks depending on the instrument configuration. For example, when EXT FM is selected, the FPGA reads digitized data from the ADC (U502) which digitizes the rear panel modulation input, then offsets, scales, and up-samples that data, and applies the result to the RF DDS's (U605) parallel input to frequency modulate the RF synthesizer's frequency reference. Another example: When the instrument is set to provide a wide span frequency ramp (Sweep, triangle, with a set modulation rate and modulation deviation) the FPGA is configured as a DDS to provide addresses that walk through a ramp of frequency values at a precise rate and provides interpolated frequency values to the parallel input of the RF DDS (U605). The FPGA will also control the values on the data bus LVL_DAC[0..13] which controls the analog signals ±RF_ATTN so as to level the amplitude of the RF output during the frequency sweep. A final example (this is a hardware provision for a future product): A user provided I/Q modulation pattern can be loaded into the static RAM. Data pairs are read from the RAM at a precise symbol rate, interpolated and up-sampled to about 125 MSPS, digitally filtered (by a root-raised cosine filter, for example), and the result applied to the dual 14-bit DAC (U513). The analog outputs from the dual DAC are filtered and applied differentially to the I/Q modulator in the RF block.

The FPGA has two clock sources whose use depends on the FPGA configuration. The PDCLK (which originates at RF DSS, U605, operating at the RF DDS frequency/4 or about 250 MHz) is used whenever the FPGA provides data to the RF DDS's parallel port. Timing is very critical in this case. The parallel data to the FPGA must arrive within a ±1 ns window with respect to the PDCLK. One of the FPGA's DCMs (Digital Clock Managers) is used to adjust the phase of the parallel output data to meet this timing requirement. The FPGA is able to measure the timing relationship between the PDCLK and the LSB of the parallel data (MD0) via IP_L32N and IP_L32P (at the upper right-hand corner of U401 on sheet 4 of 8.

The ±25 MHZ_FPGA source is used as the FPGA clock for pulse and blanking modulation. A DCM is used to multiply the 25 MHz clock to 200 MHz to provide 5 ns resolution for the pulse or blanking period and width. The FPGA can blank the RF and baseband outputs via the differential LVDS signals ±RF_BLANK and ±BB_BLANK.

The FPGA is initially programmed via the SPI from the CPU. Configurations are up-loaded to the FPGA and stored in the flash ROM during system programming at the factory. A 6-pin JTAG connector, J400, allows direct access to the FPGA for development purposes.

Modulation ADC and DACs

(Schematic 8: Mother Board 5, Modulation ADC / DACs)

There is a rear panel modulation input BNC, J500, which allows user supplied signals to modulate amplitude, frequency, or phase of the SG394 outputs. The same input can also be used for pulse and blank modulation.

In EXT PULSE or EXT BLANK modulation modes, the rear panel modulation input is discriminated by U501 to provide a digital input, EXT_TRIG, to the FPGA. Depending on the operating mode and frequency, the FPGA will use EXT_TRIG to control ±RF_BLANK and/or ±BB_BLANK to pulse or blank the signal generator's outputs.

For EXT AM, FM or ΦM, the rear panel modulation input is limited by D501 & D502, buffered by U500A, ac or dc coupled through U503, and low-pass filtered by a 1 MHz, 5^{th} order, Bessel filter (L503/L504/C511-C514). The filtered signal is buffered by U504 and digitized by U502, a 12-bit ADC operating at about 31.25 MSPS. The data from the DAC is provided to the FPGA on the 12-bit parallel data bus, ADC[0..11]. The data is offset, scaled (and linearized in the case of amplitude modulation of RF outputs) and up-sampled to modulate the amplitude, frequency or phase of the signal generator outputs.

There are four high speed (125 MSPS), high resolution (14-bit) DACs that are controlled by the FPGA. The DACs have several purposes:

1. To mimic the modulation waveform on the rear panel modulation output BNC. 2. To level the RF amplitude during sweeps. 3. To level the baseband output during sweeps,

or, to provide the I-component for I/Q modulation. 4. To level the doubler output during sweeps, or, to provide the Q-component for I/Q modulation.

All of the DACs have a similar configuration. The clock to each DAC is resynchronized to the PDCLK (from U605) to minimize sample jitter. The data to the DACs is loaded in parallel from the FPGA. The differential outputs are filtered by a Bessel low-pass filter (fc = 1 MHz for two of the DACs and fc = 10 MHz for the I/Q DACs). The filter outputs are buffered by differential line drivers with a fixed gain of ×2 and a 49.9 Ω source impedance.

RF DDS

(Schematic 9: Mother Board 6, RF Reference)

The RF DDS has two functions: To provide a reference frequency to the RF synthesizer (located in the RF block), or, in the case that the output is below 62.5 MHz, to synthesize the output directly. The RF DDS is an AD9910 (U605), which integrates a 1 GSPS NCO with a 14-bit DAC. The SFDR of the part is better than –65 dBc for output frequencies below 100 MHz. This is quite adequate for direct outputs (below 62.5 MHz) but would be unsatisfactory when multiplied up to higher frequencies. (For example, a spur would increase in magnitude by 40 dB when a reference is “multiplied” up from 40 MHz to 4 GHz.)

There is a neat trick to eliminate DDS spurs: If the DDS is programmed to divide by an integer, then the output will sample the exact same DAC levels on each cycle, and so each cycle will be the same as the others. Fourier tells us that a repetitive waveform can be represented by a fundamental sine and its harmonics; hence a *repetitive* waveform has only a fundamental and harmonics but no spurs. This is easily seen when observing a DDS output on a spectrum analyzer. As the FTW (Frequency Tuning Word) approaches a value that corresponds to division by an integer all of the spurs gather up to fit beneath either the fundamental or its harmonics.

The requirement to divide by an integer requires further thought. For a 32-bit DDS, one cycle or 360° corresponds to 2^{32} = 4,294,967,296 in the phase accumulator. Division by an integer is simple if the integer is a power of 2. For example, to divide by 16 the FTW would be 4,294,967,296/16 = 268,435,456. However, to divide by 10, the FTW would be 4,294,967,29.6. Since the FTW must be an integer, there will be a truncation error of 0.6 bits per sample, a corresponding frequency error, and spurs in the output.

To fix this (in the case of division by 10) the DDS would be programmed to use a FTW of 429,496,729 for 9 sample clocks and 429,496,735 for 1 sample clock. Doing so accumulates exactly 2^{32} in the phase accumulator after 10 sample clocks and so provides exact division by 10 with no spurs. This trick allows the RF DDS to generate a reference frequency for the RF synthesizer that has no significant spurs and so can be “multiplied” by the RF synthesizer without adding spurs to the RF output.

The clock to the RF DDS comes from a 1 GHz VCO which is phase locked to ×51 the selected 19+ MHz reference to provide precision clock rates in the ranges of 997.259 MHz ±100 ppm, 1,000.000 MHz ±10 ppm, or 1002.7467 MHz ± 100 ppm. The charge pump output from the PLL synthesizer, U604, is filtered by U603, a low-noise, high bandwidth op-amp. The loop bandwidth is about 6 kHz.

The RF DDS is programmed to divide by an integer between 10 and 50 to provide output frequencies between 20 MHz and 100 MHz. The differential outputs are filtered and buffered before being sent to the RF Block to serve as the reference frequency input to the RF synthesizer.

The RF DDS has a 16-bit parallel port to allow for agile amplitude, frequency and phase modulation. The data is passed to the RF DDS from the FPGA modulation processor. The data on the parallel input, which is synchronized to the PDCLK, can directly modulate the amplitude or phase, or may be scaled and added to the FTW for FM. The DDS may also be rapidly modulated via the profile input ports, in which case the data is synchronized to the SYNC_CLK.

The data presented to the parallel port can only be used to modulate one parameter. In the case of frequency sweeps below 62.5 MHz, the parallel data provides frequency tuning data to the RF DDS. A separate path is used to amplitude level low frequency sweeps: The differential ±BB_LEVEL signal converted to a single-ended signal by U600 and used to level the amplitude of the RF_DDS synthesizer as seen at the front panel BNC output.

RF Block and Rear-Panel Interface

(Schematic 10: Mother Board 7, Interface)

The common mode voltage on the differential output from the RF DDS is eliminated by U700, which integrates the difference between the common mode output voltage and ground. The integrated voltage is applied to the 100 Ω terminations so as to eliminate the common mode voltage.

The differential DAC output is then filtered by a Chebyshev low-pass (L700, 701, 706, 707, etc) with a cutoff frequency of 150 MHz. The output of the filter is terminated and buffered by the differential amplifier, U702. A multiplexer, U701, passes the filtered RF DDS output to the RF block as either ±RF_REF (when the set frequency is above 62.5 MHz or 93.75 MHz for the SG396) or ±BB_OUT (when the set frequency is below 62.5 MHz or 93.75 MHz for the SG396).

The connector, J701, is used to pass signals between the motherboard and two rear panel PCBs. The top rear PCB provides rear panel analog inputs that can be used to directly modulate the I/Q modulator. The multiplexers U705 and U708 select between the internal I/Q modulation sources or the external I/Q modulation sources. The rear panel PCB also provides rear panel analog outputs which are copies of the I/Q modulation.

Power Conditioning

(Schematic 11: Mother Board 8, Power Supplies)

An enclosed power supply is used to provide regulated power to the motherboard via the large header, J800. Whenever the unit is plugged into the line, the un-switched +24 V will be present. This supply is used to maintain power to the timebase (an OCXO or an optional rubidium oscillator) even when the front panel power button is “off”. When the unit is switched “on” the other supplies (±15, ±5, +3.3V) become active. The inverter that generates those other supply voltages is operated at exactly 100 kHz, synchronized by the 100 ns wide, 200 kHz PS_SYNC pulses sourced from the CPU, U300.

The grounds and power supplies are all filtered and bypassed as they come onto the motherboard. In addition, there are several regulators which provide other voltages used in the system: +20, +8.5, +3.00 (which is used as a voltage reference throughout the system), +2.5, +1.8, +1.2, and –8.5 V.

An interrupt signal, –PWR_IRQ, is generated if the +24 V supply falls below +22 V or if the power switch is turned to "off". This interrupt tell the CPU to "stand down" (in particular to not start new writes to memory) as the power supplies are about to turn "off".

Motherboard to RF Block Jumper

(Schematic 12: Mother Board to RF Jumper)

This PCB provides the interface as well as filtering the signals to minimize any interference that could impair the signal quality. Single ended control signals implement a single order RC filter; differential signals implement a common mode choke; finally, power lines implement an LC filter.

RF Output Block

The RF Output Block refers to the milled aluminum block (and its covers) which house the Type N and BNC connectors which present the main front panel outputs of the instrument. This block establishes solid RF grounds, shields the enclosed circuitry from magnetic flux generated by the power supply and from RF signals generated by the motherboard, as well as reducing the EMI from and the susceptibility of the enclosed circuitry.

There are two circuit boards inside the RF block. Facing the front of the instrument, the PCB on the right holds the RF synthesizer and provides connections to the motherboard via a 34-pin jumper board. The PCB on the left connects to the RF synthesizer and amplifies or attenuates the signal from the RF synthesizer. Signals on the Type N connector cover an amplitude range from –107 dBm to +13 dBm for signals from 950 kHz to 2.025, 4.050, or 6.075 GHz. The output board also provides outputs on the BNC with an amplitude range from 1 mV_{rms} to 1 V_{rms} from dc to 62.5 MHz.

RF Synthesizer

(Schematic 13: SG394 Synthesizer 1, 2-4 GHz and Control)
(Schematic 15: SG396 Synthesizer 1, 3-6 GHz and Control)

Control signals, frequency references, and power supplies are passed from the motherboard via a small jumper board to the RF synthesizer on J101. Many of the control signals flow through to the output amplifier/attenuator board via J100. The ±8.5 V power supplies are re-regulated to ±5_SYN supplies by U100 and U111. Differential blanking signals, ±RF_BLANK and ±BB_BLANK are converted to CMOS levels by U117 and U118. Serial SPI data is clocked into the shift registers U112 and U113 to provide various control signals.

For output frequencies below 62.5 MHz the RF DDS direct output, ±BB_OUT, is used as the source frequency output. The differential signals are passed to the output board for conditioning before being applied to the output BNC connector. The differential signals are also buffered by U119 to provided sine wave outputs for Type N.

The RF synthesizer consists of a 1900-4100 MHz VCO (3 GHz to 6 GHz for the SG396), U105, which is phase locked by U107 to the RF reference (±RF_REF) from the motherboard. The differential RF reference is transformer coupled into the 100 MHz Butterworth low-pass filter (L102, C125 & C126) which is terminated by R116. The 3 V_{PP} reference is ac coupled into the PLL synthesizer's reference input into via C123. The charge pump output of the PLL synthesizer is conditioned by the loop filter, U104. The loop bandwidth is about 100 kHz for the typical phase comparison frequency of 25 MHz. The bandwidth of the loop filter, which is set to be roughly proportional to the phase comparison frequency, is adjustable by the switches U108A-D.

The output of the RF VCO is ac coupled into a high speed PECL fanout, U106. There are two sets of outputs from U106. The first output, ±TOP_OCT, is the differential top octave output for the frequency synthesizer. The other output is used as feedback to the PLL synthesizer and to control the 50/50 symmetry of the top octave output.

The symmetry control is maintained by the differential integrator, U109. If +TOP_OCT spends more time high than –TOP_OCT, the inverting input to the integrator will ramp up, causing the non-inverting output of the integrator to ramp down, reducing the dc voltage at the non-inverting input of the fanout buffer, causing +TOP_OCT to ramp down, returning the symmetry of ±TOP_OCT to 50/50.

RF Dividers and Selectors

(Schematic 14: SG394 Synthesizer 2, Dividers and LPF)
(Schematic 16: SG396 Synthesizer 2, Dividers and LPF)

The ±TOP_OCT PECL signals are fanned out by U200. Both outputs of the fanout are source-terminated with 50 Ω and can be made active by grounding the string of three series 50 Ω resistors on the open emitter outputs. (Pulling up these resistors to +3.3V turns "off" the corresponding open-emitter output.)

For outputs between 2 GHz and 4 GHz (3 GHz and 6 GHz for the SG396), –EN_RF0 is set low, enabling the top-half of the fanout U200. One of the differential outputs is selected by the RF multiplexer, U216, to drive the rear panel Option 1 & Option 2 via J201 (the SMA connector in the side of the RF Block). The other differential output of the fanout is used for the top octave output. This signal is given some high frequency pre-emphasis by the stubbed attenuator (R205-207), amplified by U201, then low-pass filtered by U202 (to remove the harmonics of the square wave) to provide a 2 GHz-4 GHz sine wave for RF multiplexer, U211, which passes the sine wave to the output amplifier/attenuator board via the RF feed-thru, J200.

For outputs in the five octaves below the RF VCO, the control line –EN_1ST_DIV is set low, enabling the bottom half of the fanout, U200. (The top half is disabled by setting –EN_RF0 high.) This also enables the digital divider, U206, which will provide outputs via the gate U205 for outputs between 1 GHz and 2 GHz (1.5 GHz and 3 GHz for the SG396). Other dividers (U209, 212, 215, 218) are enabled for lower octaves. As before, each differential square wave source has a 50 Ω source impedance, with one-half of the differential pair being passed directly to the RF multiplexer, U216, while the other half is low-pass filtered to provide a sine to the other RF multiplex, U211. Unused dividers are disabled to eliminate sub-harmonic distortion.

The RF multiplexers (U211 & U216) are non-reflective multiplexers and so unselected inputs are terminated via 50 Ω to ground. These RF multiplexers operate with a VEE of –5 V_{DC} and so it is necessary to translate the control signals to swing between ground and –5 V_{DC}. A triple 1:2 analog switch, U213, is used to translate CMOS control signals to the 0 V/ –5V levels.

RF I/Q Modulator, Amplifiers and Attenuators

(Schematic 17: SG394 Output 1, Attenuation & Controls)
(Schematic 20: SG396 Output 1, Attenuation & Controls)

The PCB on the left side of the RF Block I/Q modulates, amplitude modulates, amplifies, and attenuates the selected RF signal before passing it out the front panel connectors. This PCB receives power, control and differential modulation signals from the RF synthesizer PCB via J101. The selected RF signal is passed from the RF synthesizer to this PCB via the RF feed-thru, J100.

The signal path toward the Type N connector begins at J100. If the carrier frequency is between 400 MHz and 4.05 GHz (6 GHz for the SG396), the signal at J100 may be multiplexed to the I/Q modulator, U110. If the signal is outside of this range, or if I/Q modulation is not enabled, the SPDT switches, U103 and U104, bypass the I/Q modulator.

The carrier signal is ac coupled into the I/Q modulator via C116. The modulator converts the input signal into two phase-shifted square waves, I & Q. The each square wave can be amplitude modulated the corresponding differential modulation inputs, ±I_MOD and ±Q_MOD. The amplitude modulated components are summed together and appear at the RF output. The RF output is attenuated (to match its input carrier level), given high frequency pre-emphasis (via the stubs in the pi-attenuator legs) and low pass filtered (to remove harmonics) and directed back into the RF signal path by the SPDT switch, U104.

Two RF voltage variable attenuators (VVA), U111 & U112, are used to amplitude level or amplitude modulate the RF signal. The attenuation is controlled by a dc voltage applied to the V1 input of each VVA. The attenuation increases as V1 becomes more negative. The attenuation characteristic is not linear, which requires compensation to the control voltage, especially for deep amplitude modulation.

The attenuator control voltage is sourced from ±RF_ATTN, which is converted to a single-ended voltage by U114 and low-pass filtered (for noise reduction) by L106 and C128. These attenuators are used to provide attenuation between the digital attenuator steps and to correct for the differential non-linearity of the digital attenuators. They are also used to amplitude level sweeps and for amplitude modulation.

The first of three RF gain blocks is U109. The gain of this amplifier is +15 dB. It is an ac amplifier which requires a dc current bias be applied to its output. It is important that the dc bias network be high impedance over the operating range (1 MHz to 6 GHz) and that it not have any significant resonances. This is achieved with three series inductors, with staggered self resonant frequencies, and with parallel damping resistors. This method is used on all the gain blocks in the signal chain.

The output from the first gain block is ac coupled into the first of five digital attenuators, U107. The digital attenuators are controlled in 0.5 dB steps from 0 dB to 31.5 dB. They are powered from +5 V and are controlled by the SPI interface. The power supplies and SPI signals are filtered from stage-to-stage to reduce signal and noise feed-through.

RF Output Attenuators

(Schematic 18: SG394 Output 2, RF Stage)
(Schematic 21: SG396 Output 2, RF Stage)

To achieve an amplitude dynamic range of 120 dB (from –107 dBm to +13 dBm) over 6 GHz requires extraordinary care in the design, layout and grounding of the circuit. In particular, it is important that there be no signal paths which "go around" the intended signal path. For example, if –100 dB of a signal can go around the attenuator chain via a control line or power line, then the effective attenuation range will be limited.

RF grounding is reestablished in each of the four stages shown on Sheet 2 of 3, with both the power supplies and serial control lines being filtered at each stage before being passed to the next. Physically, the circuit layout is within a series of "rooms", with good ground connections, and shielded from other parts of the circuit by the milled aluminum block.

The RF signal chain continues with the output of the attenuator on the previous page being applied to the first attenuator, U201, on the next page. The signal chain continues with an amplifier, two attenuators, another amplifier, and a final output attenuator. The final amplifier, U206, has higher gain and can provide more output power than the other gain blocks. It also requires more bias current.

BNC Output

(Schematic 19: SG394 Output 3, BNC)
(Schematic 22: SG396 Output 3, BNC)

The differential outputs, ±BB_OUT, are passed from the RF DDS on the motherboard to the output board via the RF synthesizer board. These differential signals can be blanked by the dual differential switches U301 & U302 by BB_BLANK_CTL.

±BB_OUT are converted to a single-ended signal by U303, whose output is low-pass filtered (to reduce noise bandwidth and reduce high frequency spurs) by L303, C305 & C306. The signal is then attenuated by the digitally controlled attenuator, U304, which can provide 0 to 31 dB of attenuation in 1 dB steps. (Finer steps are provided by the RF DDS, whose amplitude can be set with 16-bit of resolution.) A fixed 30 dB of attenuation is provided by R302/306/307 under the control of the switch U305. The high bandwidth switches, U301, U302 and U305, are operated from ±3 V, and so their control lines are level shifted by U100 and U101 to ±3 V.

An output amplifier, U300B, buffers the attenuator output and provides a gain of ×3. A final output driver, U300A, sums in an offset voltage, BB_OFFSET, and drives the output BNC via a 49.9Ω resistor. The BNC output is sampled for measurement by the CPU via the filtered signal BB_MON.

Power Supply

(Schematic 23: Power Supply)

The power supply for the unit is contained in a separate shielded enclosure. The unit accommodates universal input voltages (90-264 V_{AC}, 47-63 Hz) and provides a variety of dc voltages to the motherboard (+24, +15, +5, +3.3, –5, –15 V.) The unit will lock its dc-dc converter to a 200 kHz sync signal provided by the motherboard. The unit also has a thermostatically controlled fan whose speed increases with increasing temperature.

An OEM power supply (CUI Inc VSBU-120-24) provides up to 5 A at +24 V from the line voltage input. This power supply is "on" whenever the line voltage is present, supplying +24 V to the motherboard to power the timebase (either the standard ovenized crystal or optional rubidium oscillator.) The +24 V supplied to the motherboard is filtered by L1 & C1 to remove ripples from the OEM power supply. The OEM supply also provides +24 V for a dc-dc converter to generate the other regulated voltages used in the system. The dc-dc converter and fan are "on" only when the front panel power button is pressed "in".

The dc-dc converter is disabled when the –DISABLE (pin 8 on the motherboard interface) is held low. When –DISABLE is released the switching power supply controller, U7, generates complementary square waves at about 100 kHz to drive the MOSFETs (Q2 & Q3) into conduction during alternate half-cycles. The MOSFETs drive the primary of a transformer. The secondary voltages are rectified, filtered, and regulated to provide the +15, +5, +3.3, –5, & –15 V system voltages.

The regulated outputs have Schottky diodes on their outputs which prevent the power supplies from being pulled to the wrong polarity by loads which are connected to other supplies with opposite polarities. This is most important during start-up and to avoid SCR action in CMOS ICs in the case that one of the supplies should fail.

A thermostatic fan speed control helps to regulate the operating temperature of the entire instrument. This circuit uses an LM45 (10mV/deg C) as a temperature sensor. The output from the temperature sensor is offset, multiplied, and limited to a 0-15 V range. This voltage is drives a 12 V medium speed fan via the emitter follower, Q1.

Rear-Panel Boards

There are two rear panel PCBs which interface to the mother board via the Jumper PCB (Schematic 24: Rear Panel Option Jumper).

I/Q Modulator

(Schematic 25: I/Q Modulator)

The rear panel I/Q modulation inputs allow the user to modulate the amplitudes of the in-phase and quadrature components of RF carriers between 400 MHz and 6.075 GHz with analog signals.

The I & Q channels use the same circuit configuration. The quadrature component, ±0.5 V or 1 Vpp, is applied to the rear panel BNC connector, J2. The input signal is terminated into 50 Ω by the parallel combination of the 52.3 Ω input termination in parallel with the 1125 Ω input impedance to the differential amplifier U4. The differential outputs drive a differential transmission line returning to the motherboard via 49.9 Ω resistors and J4.

Overloads are detected at the output of the differential amplifier by the fast window comparator, U2A&B. If an overload is detected at either the I or Q inputs, the differential signal ±OVLD_I/Q will be asserted and passed to the motherboard via J4 for detection by the CPU.

This option also provides rear panel I/Q modulation outputs. The modulation signals may originate from the rear panel modulation input or from the internal, dual, arbitrary modulation generator. The modulation signals from the motherboard, ±I_OUT and ±Q_OUT are received by U1 and U5 and converted to single-ended signals which drive the BNC outputs via 49.9 Ω resistors. These outputs are intended to drive 50 Ω loads to ±0.5 V or 1 V_{pp}.

Symbol Clock and Event Output

(Schematic 26: Symbol Clock and Event Markers)

This rear panel PCB provides a Symbol Clock and three Event Outputs. The symbol clock, whose rising edge is synchronous with the optimum sampling time for I/Q modulation symbols, is also used to resynchronize the event outputs.

The rear panel Sync & Event PCB has two connections to the motherboard: the vertical jumper PCB (for power supplies and the differential analog signal, DBL_LEVEL, which is repurposed to provide a sample rate clock for modulation by an audio waveform), and, four LVDS signal via a short CAT-5 cable.

Eight control bits, transmitted via the SPI, are latched into U2. The symbol clock is sourced from either the comparator (U3) or from the LDVS receiver, U8, under control of the bit -SEL_AUDIO_CLK. Other control bits are used to set or clear the event outputs. The output drivers provide fast pulses with 50 Ω source impedance.

Timebase Options

(Schematic 27: Timebase Adaptor Interface)

The standard timebase is an OCXO (SRS p/n SC-10-24-1-J-J-J-J). A rubidium frequency standard (SRS p/n PRS10) may be ordered as Option 4. Both timebases are held by the same mechanical bracket and connected to the system using the same adapter PCB.

The adapter PCB schematic is quite simple: J1 is the connector to the OCXO option, J2 is the connector to the rubidium option, and J3 is the connector to the main PCB. The op amp U1 is used to scale the 0-4.095 V_{DC} frequency calibration voltage (CAL_OPT) to 0-10 V_{DC} for the OCXO or 0-5 V_{DC} for the rubidium. The logic inverter, U2, is used to invert the logic levels for the RS-232 communication between the microcontroller on the main PCB and the PRS10 rubidium frequency standard.

Appendix A : Rational Approximation Synthesis

The SG390 Series RF synthesizers use a new approach to synthesizer design that provides low phase noise outputs with virtually infinite frequency resolution and agile modulation characteristics. The technique is called Rational Approximation Frequency Synthesis. Some details of the technique will help users to understand the performance capabilities of the instruments.

Phase Lock Loop Frequency Synthesizers

Phase lock loop (PLL) frequency synthesizers are a cornerstone technology used in every modern communication device and signal generator. The classical PLL block diagram is shown in Diagram 1.

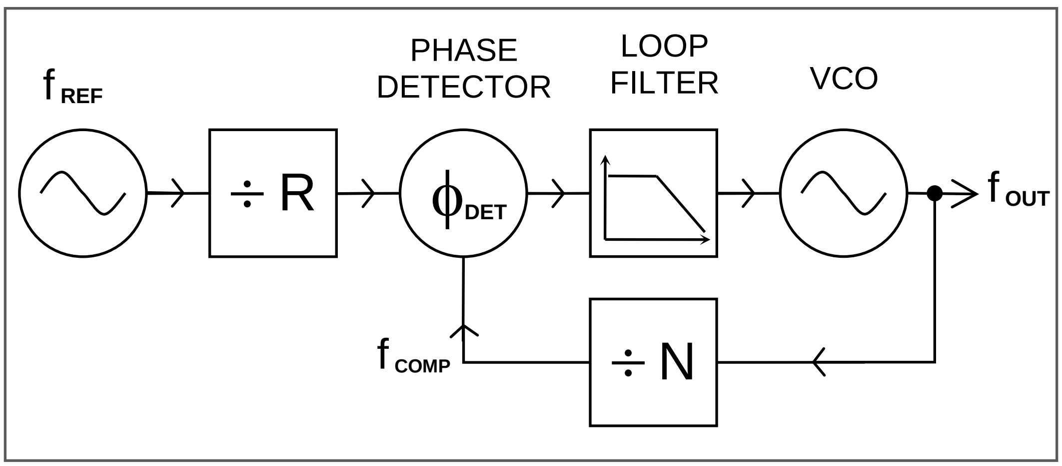


Diagram 1: Classical "Integer-N" PLL Frequency Synthesizer

The purpose of the PLL synthesizer is to generate precise output frequencies that are locked to a reference frequency. As shown in Fig 1, the reference frequency, f_{REF}, is divided by the integer R and the voltage controlled oscillator (VCO) output, f_{OUT}, is divided by the integer N. A phase detector compares the phase of the divided frequencies. The phase detector output is low-pass filtered and used to control the frequency of the VCO so that f_{OUT} / N is equal to f_{REF} / R, hence $f_{OUT} = N \times f_{REF} / R$.
A numerical example will help to illustrate the operation and design trade-offs of the PLL. Suppose f_{REF} = 10 MHz and R = 1000. If N = 10,000 then the output frequency, $f_{OUT} = N \times f_{REF} / R$ = 100 MHz. As N is changed from 10,000 to 10,001 to 10,002, f_{OUT} will change from 100.00 MHz to 100.01 MHz to 100.02 MHz. This PLL synthesizer has a phase comparison frequency, and a channel spacing, of f_{REF} / R = 10 kHz.

Phase Noise

Diagram 2 shows a typical phase noise plot for a 100 MHz PLL synthesizer. The phase noise plot shows the noise power in a 1 Hz sideband as a function of frequency offset from the carrier. There are three dominate sources of phase noise: The reference, the phase detector, and the VCO. The frequency reference dominates the noise close to the carrier but falls off quickly at large offsets. The phase detector noise floor is relatively flat vs. frequency but decreases with increasing phase comparison frequency. In fact, the phase detector noise decreases by about 10 dB / decade, hence is about 30 dB lower for phase comparisons at 10 MHz vs. 10 kHz. Finally, the VCO phase noise will dominate at offset frequencies beyond the loop bandwidth. A high phase comparison frequency, hence low R & N divisors, is required for a low phase noise design.

In a properly designed PLL the output noise tracks the reference at low offsets, matches the phase detector noise at intermediate offsets, and is equal to the VCO noise at offsets beyond the PLL loop bandwidth. Careful attention to the loop filter design is also required to achieve the total noise characteristic shown in Diagram 2.

In addition to broadband noise there will be discrete spurious frequencies in the phase noise spectrum. A dominant spur is often seen at the phase comparison frequency. It is easier to reduce this spur in a filter when the phase comparison frequency is high.

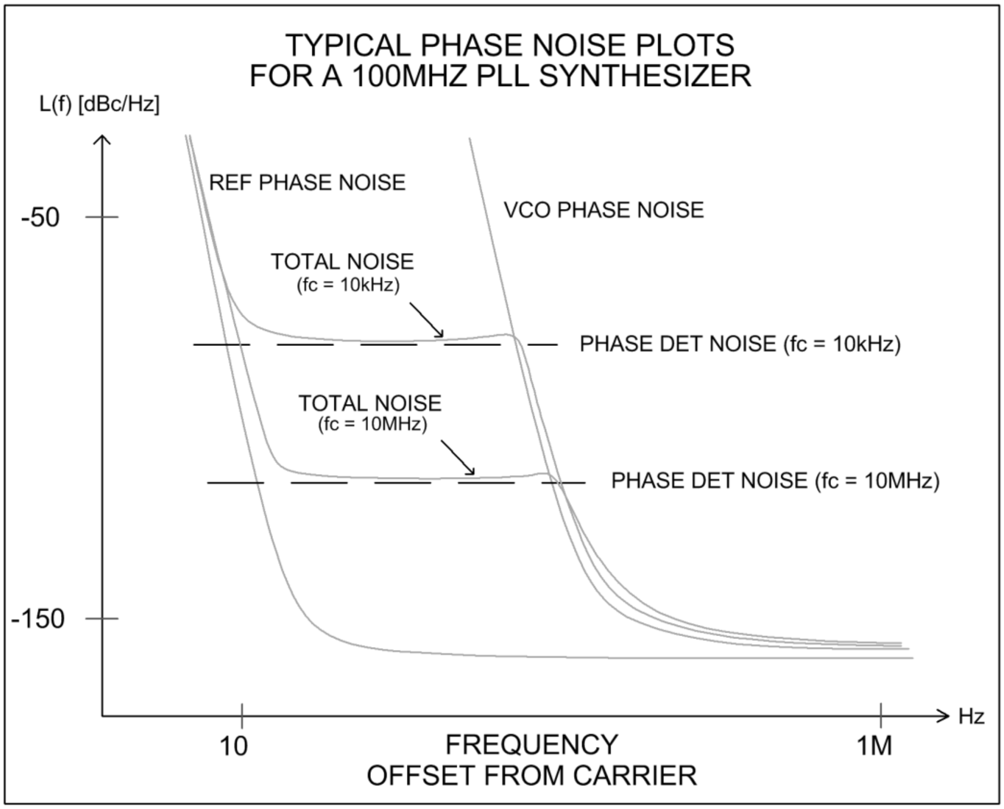


Diagram 2: Typical Phase Noise Spectrum for a 100 MHz PLL Frequency Synthesizer

Increasing Frequency Resolution

A frequency resolution of 10 kHz, or channel spacing of 10 kHz, is adequate in many communications applications but a higher resolution is desired in test and measurement applications. The simplest way to increase the frequency resolution is to increase the value of the R divider. In the above example, if R were increased from 1000 to 10,000 the frequency resolution (channel spacing) would be increased from 10 kHz to 1 kHz. However, there are several serious drawbacks to this strategy. As the R divider is increased the phase comparison frequency is decreased leading to higher phase detector noise, a reduction in the loop bandwidth, and increased settling times. *Increasing R will achieve high frequency resolution at the cost of a noisy output that takes a long time to settle.*

A Note on Fractional-N Synthesis

Another strategy to increase resolution without decreasing the phase comparison frequency is to use a Fractional-N synthesizer. In these synthesizers the value of N is modulated so that its average value can be a non-integer. If N averages to 10,000.1 then the output frequency, $f_{OUT} = N \times f_{REF} / R = 100.001$ MHz. The frequency resolution has been improved to 1 kHz. However, modulating the N value creates spurs in the VCO output. Dithering techniques are able to spread most of the spur energy into broadband noise, but the remaining noise and spurs is problematic in some applications.

About YIG Oscillators

One work-around to the trade-off between high resolution and reduced phase comparison frequency (and so higher phase noise) is to use a YIG oscillator. YIGs are extremely good VCOs due to the extremely high Q of their resonator which consists of a sub-millimeter yttrium-iron-garnet sphere tuned by a magnetic field. However, YIGs have their drawbacks including high power, slow tuning, susceptibility to environmental magnetic fields, and high cost. The SG390 Series of RF synthesizers achieve YIG performance from electrically tuned VCOs by arranging a very high phase comparison frequency.

A New Approach

A new approach to synthesizer design provides high frequency resolution, fast settling, and low phase noise. This new approach is called *Rational Approximation Frequency Synthesis*. (A rational number is a number which is equal to the ratio of two integers.) The approach has been overlooked as it relies on some surprising results of rather quirky arithmetic which abandons neat channel spacing in exchange for a much better performing PLL synthesizer.

Once again, a numerical example will be useful. Suppose we want to use our PLL synthesizer to generate 132.86 MHz. We could do that by setting R = 1000 and N = 13,286. With f_{REF} = 10 MHz we have $f_{OUT} = N \times f_{REF} / R$ = 132.86 MHz. The phase comparison frequency is 10 kHz and so the PLL loop bandwidth, which is typically 1 / 20th of the phase comparison frequency, would be only about 500Hz.

There's another way to synthesize 132.86 MHz (or at least very close to it.) Suppose we set R = 7 and N = 93. Then $f_{OUT} = N \times f_{REF} / R$ = 132.857142 MHz, which is only 21.5 ppm below the target frequency (Hence the term "Rational Approximation". Of course, increasing the reference frequency by 21.5 ppm will produce the target frequency exactly, as will be described.) Momentarily suspending the question of the general applicability of this approach, the positive benefit is clear: The phase comparison frequency is now 10 MHz / 7 = 1.42 MHz which is 142 times higher than that provided by the classical PLL with a 10 kHz channel spacing. This allows a PLL bandwidth which is also 142 times wider. The higher comparison frequency of this PLL will provide faster settling, lower phase noise, and an easily removed reference spur which is 1.42 MHz away from the carrier.

Several questions arise.

1. Is this approach generally applicable, that is, can *small* values for R & N always be found to produce an output close to any desired frequency?
2. Is there a method to find the smallest values for R & N?
3. Can the output frequency be made exact (not just "close to") the desired frequency.

The answer to all three questions is "Yes". Details are well illustrated by a real-world example.

An Example

Diagram 3 shows a PLL synthesizer that can generate outputs anywhere in the octave between 2 GHz and 4 GHz. Lower frequencies are easily generated by binary division of this output. This example uses an Analog Devices dual-modulus PLL frequency synthesizer, the ADF4108. A dual modulus N counter is a high-speed divider which divides by a prescaler value, P, or by P+1 under the control of two registers named A & B. The dual modulus N-divider adds a bit of numerological quirkiness as there are restrictions on the allowed values for A & B as detailed in Diagram 3. The ADF4108 also requires that the phase comparison frequency be less than 104 MHz. The reference frequency input in this example is 200 MHz.

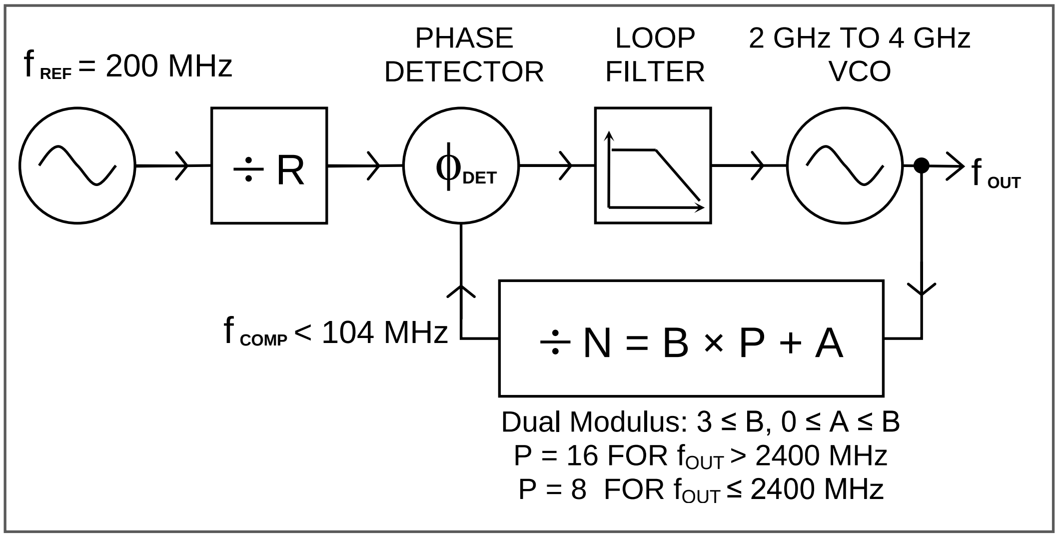


Diagram 3: A Rational Approximation Frequency Synthesizer

One curious aspect of Rational Approximation Frequency Synthesis is that it is not obvious how to choose the values for R & N. There are mathematical techniques for rational fraction approximation however brute enumeration of the possibilities may also be used. For example, R & N can be found by starting with the lowest allowed value for R and testing to see if there is an allowed value for N which gives a result, $f_{OUT} = N \times f_{REF} / R$, which is within some error band (say, ±100 ppm) of the desired frequency. Luckily, these computational requirements are modest. The required calculations can be performed on a typical microcontroller in under a millisecond.

The largest phase comparison frequencies are achieved when there are many numeric choices available to improve the chance that a particular ratio of integers can be found which will be within the error band of the desired result. This is done three ways. First, allow a large error band. (An error band of ±100 ppm is typical because a fundamental mode crystal oscillator, which is used to clean-up the reference source, can be tuned over ±100 ppm.) Second, use a high frequency reference oscillator. Third, provide a second reference, detuned slightly from the first, to provide additional numeric choices.

To ascertain how well Rational Approximation Frequency Synthesis works for the example in Diagram 3, a computer program was written to compute the R & N values for 10,000 random frequencies in the octave band between 2 GHz and 4 GHz. Using a single reference source at 200 MHz, and an allowed error band of ±100 ppm, the average phase comparison frequency was 9.79 MHz and the worst case phase comparison frequency was 400 kHz.

When a second reference frequency was available (at 201.6 MHz, as determined by trial and error while searching for the highest worst-case phase comparison frequency) the average phase comparison frequency increased to 12.94 MHz and the worse case phase comparison frequency increased to 2.35 MHz (a six-fold increase.)

Elimination of Error

Rational Approximation Frequency Synthesis provides a fast settling, low phase noise, and spur-free output, but with a troubling "error band" of typically ±100 ppm. To eliminate this error it will be necessary to provide a low noise reference that is tunable over ±100 ppm with very high resolution. A VCXO phase locked with narrow bandwidth to a DDS source may be used for this reference. A 48-bit DDS provides a frequency resolution of $1{:}2\times10^{-14}$ and the VCXO effectively removes all of the DDS spurs.

A tunable reference source is shown in Diagram 4. A 10 MHz timebase is multiplied in the DDS to 100 MHz. The DDS is programmed to generate an output within ±100 ppm of 18.1818 MHz. The VCXO is phase locked to the DDS output with a 100Hz bandwidth. The clean 18.1818 MHz VCXO output is used as a source for an 11× multiplier to produce a 200 MHz reference tunable over ±100ppm with a frequency resolution of $1{:}2\times10^{-14}$. This tunable frequency reference is used as the reference for the Rational Approximation Frequency Synthesizer, eliminating the error band inherent in the technique.

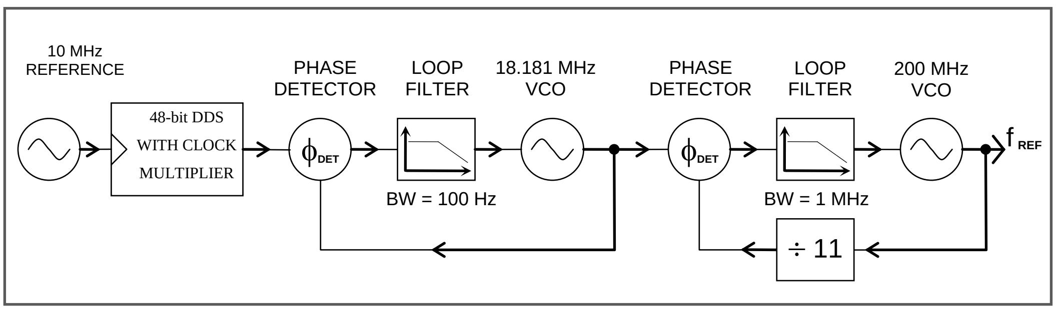


Diagram 4: Tunable (±100 ppm) 200 MHz Reference

Conclusion

A new method for the operation of classical integer-N PLL frequency synthesizers has been described. The method, Rational Approximation Frequency Synthesis, allows for operation at much higher phase comparison rates than the classical approach. The higher phase comparison rates allow wider PLL bandwidth to provide faster settling, lower phase noise, and spur-free outputs with virtually infinite frequency resolution.

Appendix B : Parts List

Front Display (Assemblies 320 & 321)

Ref	Value	Description	SRS P/N
C1	4.7U - 16V X5R	Ceramic, 16V, 1206, X5R	5-00611
C2	100000P	Capacitor, 0603, X7R	5-00764
C3	100000P	Capacitor, 0603, X7R	5-00764
C4	100000P	Capacitor, 0603, X7R	5-00764
C5	100000P	Capacitor, 0603, X7R	5-00764
C6	100000P	Capacitor, 0603, X7R	5-00764
C7	100000P	Capacitor, 0603, X7R	5-00764
C8	100000P	Capacitor, 0603, X7R	5-00764
C9	100000P	Capacitor, 0603, X7R	5-00764
C10	100000P	Capacitor, 0603, X7R	5-00764
C11	100000P	Capacitor, 0603, X7R	5-00764
D1	GREEN	LED, T-3/4	3-00424
D2	GREEN	LED, T-3/4	3-00424
D3	GREEN	LED, T-3/4	3-00424
D4	GREEN	LED, T-3/4	3-00424
D5	GREEN	LED, T-3/4	3-00424
D6	GREEN	LED, T-3/4	3-00424
D7	GREEN	LED, T-3/4	3-00424
D8	GREEN	LED, T-3/4	3-00424
D9	RED	LED, T-3/4	3-00425
D10	GREEN	LED, T-3/4	3-00424
D11	GREEN	LED, T-3/4	3-00424
D12	GREEN	LED, T-3/4	3-00424
D13	GREEN	LED, T-3/4	3-00424
D14	GREEN	LED, T-3/4	3-00424
D15	GREEN	LED, T-3/4	3-00424
D16	GREEN	LED, T-3/4	3-00424
D17	GREEN	LED, T-3/4	3-00424
D18	GREEN	LED, T-3/4	3-00424
D19	GREEN	LED, T-3/4	3-00424
D20	GREEN	LED, T-3/4	3-00424
D21	GREEN	LED, T-3/4	3-00424
D22	GREEN	LED, T-3/4	3-00424
D23	GREEN	LED, T-3/4	3-00424
D24	GREEN	LED, T-3/4	3-00424
D25	GREEN	LED, T-3/4	3-00424
D26	GREEN	LED, T-3/4	3-00424
D27	GREEN	LED, T-3/4	3-00424
D28	GREEN	LED, T-3/4	3-00424
D29	GREEN	LED, T-3/4	3-00424
D30	GREEN	LED, T-3/4	3-00424
D31	GREEN	LED, T-3/4	3-00424
D32	GREEN	LED, T-3/4	3-00424
D33	GREEN	LED, T-3/4	3-00424
D34	GREEN	LED, T-3/4	3-00424
D35	GREEN	LED, T-3/4	3-00424
D36	GREEN	LED, T-3/4	3-00424
D37	GREEN	LED, T-3/4	3-00424
D38	GREEN	LED, T-3/4	3-00424
D39	GREEN	LED, T-3/4	3-00424
D40	GREEN	LED, T-3/4	3-00424
D41	GREEN	LED, T-3/4	3-00424
D42	GREEN	LED, T-3/4	3-00424
D43	GREEN	LED, T-3/4	3-00424
D44	GREEN	LED, T-3/4	3-00424
D45	GREEN	LED, T-3/4	3-00424
D46	GREEN	LED, T-3/4	3-00424
D47	RED	LED, T-3/4	3-00425
JP1	9 PIN	Connector	1-01308
PC1	SG385 F/P	Fabricated component	7-02099
Q1	MBT3906DW1	Dual PNP Transistor	3-01419
Q2	MBT3906DW1	Dual PNP Transistor	3-01419
Q3	MBT3906DW1	Dual PNP Transistor	3-01419
Q4	MBT3906DW1	Dual PNP Transistor	3-01419
Q5	MBT3906DW1	Dual PNP Transistor	3-01419
Q6	MBT3906DW1	Dual PNP Transistor	3-01419
Q7	MBT3906DW1	Dual PNP Transistor	3-01419
Q8	MBT3906DW1	Dual PNP Transistor	3-01419
Q9	MBT3906DW1	Dual PNP Transistor	3-01419
Q10	MBT3906DW1	Dual PNP Transistor	3-01419
Q11	MBT3906DW1	Dual PNP Transistor	3-01419
Q12	MBT3906DW1	Dual PNP Transistor	3-01419
Q13	MBT3906DW1	Dual PNP Transistor	3-01419
Q14	MBT3906DW1	Dual PNP Transistor	3-01419
Q15	MBT3906DW1	Dual PNP Transistor	3-01419
Q16	MBT3906DW1	Dual PNP Transistor	3-01419
R1	49.9K	Resistor, 0603, Thin Film	4-02320
R2	20.0K	Resistor, 0603, Thin Film	4-02282
R3	499	Resistor, 0603, Thin Film	4-02128
R4	499	Resistor, 0603, Thin Film	4-02128
R5	100	Resistor, 0603, Thin Film	4-02061
R6	100	Resistor, 0603, Thin Film	4-02061
RN1	8 X 680	Resistor network	4-02531
RN2	8 X 680	Resistor network	4-02531
RN3	8 X 680	Resistor network	4-02531
RN4	8 X 680	Resistor network	4-02531
RN5	8 X 680	Resistor network	4-02531
RN6	8 X 680	Resistor network	4-02531
RN7	8 X 680	Resistor network	4-02531
RN8	8 X 680	Resistor network	4-02531
RN9	8 X 680	Resistor network	4-02531
RN10	8 X 680	Resistor network	4-02531
RN11	8 X 680	Resistor network	4-02531
RN12	8 X 680	Resistor network	4-02531
RN13	8 X 680	Resistor network	4-02531
RN14	8 X 680	Resistor network	4-02531
RN15	8 X 680	Resistor network	4-02531
RN16	8 X 680	Resistor network	4-02531
RN17	8X100	Resistor network	4-02497
RN18	8X100	Resistor network	4-02497
RN19	8X100	Resistor network	4-02497
RN20	8X100	Resistor network	4-02497
RN21	8X100	Resistor network	4-02497
RN22	8X100	Resistor network	4-02497
RN23	8 X 680	Resistor network	4-02531
RN24	8 X 680	Resistor network	4-02531
RN25	10KX4D	Resistor network	4-00912
RN26	10KX4D	Resistor network	4-00912
RN27	10KX4D	Resistor network	4-00912
RN28	10KX4D	Resistor network	4-00912
RN29	10KX4D	Resistor network	4-00912
RN30	10KX4D	Resistor network	4-00912
RN31	10KX4D	Resistor network	4-00912
RN32	10KX4D	Resistor network	4-00912
RN33	10KX4D	Resistor network	4-00912
U1	HDSP-A101	Seven Segment Display	3-00290
U2	HDSP-A101	Seven Segment Display	3-00290
U3	HDSP-A101	Seven Segment Display	3-00290
U4	HDSP-A101	Seven Segment Display	3-00290
U5	HDSP-A101	Seven Segment Display	3-00290
U6	HDSP-A101	Seven Segment Display	3-00290
U7	HDSP-A101	Seven Segment Display	3-00290
U8	HDSP-A101	Seven Segment Display	3-00290
U9	HDSP-A101	Seven Segment Display	3-00290
U10	HDSP-A101	Seven Segment Display	3-00290
U11	HDSP-A101	Seven Segment Display	3-00290
U12	HDSP-A101	Seven Segment Display	3-00290
U13	HDSP-A101	Seven Segment Display	3-00290
U14	HDSP-A101	Seven Segment Display	3-00290
U15	HDSP-A101	Seven Segment Display	3-00290
U16	HDSP-A101	Seven Segment Display	3-00290

U17	74HC595ADT	Shift Register/Latch	3-00672
U18	74HC595ADT	Shift Register/Latch	3-00672
U19	74HC595ADT	Shift Register/Latch	3-00672
U20	74HC595ADT	Shift Register/Latch	3-00672
U21	74HC595ADT	Shift Register/Latch	3-00672
U22	74HC595ADT	Shift Register/Latch	3-00672
U23	74HC595ADT	Shift Register/Latch	3-00672
U24	74HC595ADT	Shift Register/Latch	3-00672
U25	74HC595ADT	Shift Register/Latch	3-00672
U26	74HC595ADT	Shift Register/Latch	3-00672
U27	74HC595ADT	Shift Register/Latch	3-00672
U28	74HC595ADT	Shift Register/Latch	3-00672
U29	74HC595ADT	Shift Register/Latch	3-00672
U30	74HC595ADT	Shift Register/Latch	3-00672
U31	74HC595ADT	Shift Register/Latch	3-00672
U32	74HC595ADT	Shift Register/Latch	3-00672
U33	74LVC3G34DCTR	Triple non-inverting buffer	3-01852
U34	74LVC2G08DCT	Single 2-input AND gate	3-01656
U35	74LVC2G04	Dual inverting buffer	3-01968
U36	74HC595ADT	Shift Register/Latch	3-00672
U37	74HC595ADT	Shift Register/Latch	3-00672
U38	74HC595ADT	Shift Register/Latch	3-00672
U39	74HC595ADT	Shift Register/Latch	3-00672
U40	74HC595ADT	Shift Register/Latch	3-00672
U41	74HC595ADT	Shift Register/Latch	3-00672
U42	74HC595ADT	Shift Register/Latch	3-00672
U43	74HC595ADT	Shift Register/Latch	3-00672
U44	74LVC1G125DBV	Single tri-state buffer	3-01886
U45	74HC165	Shift register, PI/SO	3-01969
U46	74HC165	Shift register, PI/SO	3-01969
U47	74HC165	Shift register, PI/SO	3-01969
U48	74HC165	Shift register, PI/SO	3-01969
U49	74HC165	Shift register, PI/SO	3-01969
U50	ADCMP371	Comparator	3-01970
Z0	PS300-40	Fabricated component	7-00217
Z1	SG386,FP LEXAN	Fabricated component	7-02330
Z2	SG382 LEXAN	Fabricated component	7-02228
Z3	4-40X1/4PP	Hardware	0-00187
Z4	SIM-PCB S/N	Label	9-01570
Z5	SG385,FR CHASSI	Fabricated component	7-02106
Z6	SG385 KEYPAD	Fabricated component	7-02115
Z7	SG384 LEXAN	Fabricated component	7-02116
Z8	4-40X1/4PF	Hardware	0-00150

Front Display EMI Filter (Assembly 324)

Ref	Value	Description	SRS P/N
C1	1000P	Capacitor, 0603, NPO	5-00740
C2	1000P	Capacitor, 0603, NPO	5-00740
C3	1000P	Capacitor, 0603, NPO	5-00740
C4	22P	Capacitor, 0603, NPO	5-00700
C5	22P	Capacitor, 0603, NPO	5-00700
C6	22P	Capacitor, 0603, NPO	5-00700
C7	22P	Capacitor, 0603, NPO	5-00700
C8	22P	Capacitor, 0603, NPO	5-00700
C9	22P	Capacitor, 0603, NPO	5-00700
C10	22P	Capacitor, 0603, NPO	5-00700
C11	22P	Capacitor, 0603, NPO	5-00700
C12	22P	Capacitor, 0603, NPO	5-00700
C13	22P	Capacitor, 0603, NPO	5-00700
C14	22P	Capacitor, 0603, NPO	5-00700
C15	22P	Capacitor, 0603, NPO	5-00700
C16	22P	Capacitor, 0603, NPO	5-00700
C17	22P	Capacitor, 0603, NPO	5-00700
J2	9 PIN R/A T-H	Connector	1-01302
J3	9P FEM/T-H	Connector	1-01303
L1	2506031517Y0	Inductor BEAD 0603	6-00759
L2	2506031517Y0	Inductor BEAD 0603	6-00759
L3	2506031517Y0	Inductor BEAD 0603	6-00759
L4	2506031517Y0	Inductor BEAD 0603	6-00759
L5	2506031517Y0	Inductor BEAD 0603	6-00759
PCB1	SG385 F/P FLTER	Fabricated component	7-02208
R1	49.9	Resistor, 0603, Thin Film	4-02032
R2	49.9	Resistor, 0603, Thin Film	4-02032
R3	49.9	Resistor, 0603, Thin Film	4-02032
R4	49.9	Resistor, 0603, Thin Film	4-02032
R5	49.9	Resistor, 0603, Thin Film	4-02032
R6	49.9	Resistor, 0603, Thin Film	4-02032
R7	49.9	Resistor, 0603, Thin Film	4-02032
R8	49.9	Resistor, 0603, Thin Film	4-02032
R9	49.9	Resistor, 0603, Thin Film	4-02032
R10	49.9	Resistor, 0603, Thin Film	4-02032
R11	49.9	Resistor, 0603, Thin Film	4-02032
R12	49.9	Resistor, 0603, Thin Film	4-02032
R13	49.9	Resistor, 0603, Thin Film	4-02032
R14	49.9	Resistor, 0603, Thin Film	4-02032
Z0	SIM-PCB S/N	Label	9-01570

Motherboard (Assemblies 322 & 323)

Ref	Value	Description	SRS P/N
C100	1000P	Capacitor, 0603, NPO	5-00740
C101	100000P	Capacitor, 0603, X7R	5-00764
C102	100000P	Capacitor, 0603, X7R	5-00764
C103	10P	Capacitor, 0603, NPO	5-00692
C104	100000P	Capacitor, 0603, X7R	5-00764
C105	.47U / 16V	Capacitor, 1206, X7R	5-00527
C106	1000P	Capacitor, 0603, NPO	5-00740
C107	.47U / 16V	Capacitor, 1206, X7R	5-00527
C108	10000P	Capacitor, 0603, X7R	5-00752
C109	10000P	Capacitor, 0603, X7R	5-00752
C110	47P	Capacitor, 0603, NPO	5-00708
C111	470P	Capacitor, 0603, NPO	5-00732
C112	10000P	Capacitor, 0603, X7R	5-00752
C113	100000P	Capacitor, 0603, X7R	5-00764
C114	10P	Capacitor, 0603, NPO	5-00692
C115	.01U	Capacitor, Metal Film	5-00052
C116	1000P	Capacitor, 0603, NPO	5-00740
C117	100P	Capacitor, 0603, NPO	5-00716
C118	100000P	Capacitor, 0603, X7R	5-00764
C119	1.0U	Capacitor, Mylar/Poly, 60V, 5%	5-00245
C120	1000P	Capacitor, 0603, NPO	5-00740
C121	100000P	Capacitor, 0603, X7R	5-00764
C122	.22U	Capacitor, Metal Film	5-00057
C123	100000P	Capacitor, 0603, X7R	5-00764
C124	.047U	Capacitor, Metal Film	5-00054
C125	100000P	Capacitor, 0603, X7R	5-00764
C126	100000P	Capacitor, 0603, X7R	5-00764
C127	10000P	Capacitor, 0603, X7R	5-00752
C128	100000P	Capacitor, 0603, X7R	5-00764
C129	.47U / 16V	Capacitor, 1206, X7R	5-00527
C130	.47U / 16V	Capacitor, 1206, X7R	5-00527
C131	.47U / 16V	Capacitor, 1206, X7R	5-00527
C132	39P	Capacitor, 0603, NPO	5-00706
C133	1000P	Capacitor, 0603, NPO	5-00740
C134	.47U / 16V	Capacitor, 1206, X7R	5-00527
C135	100000P	Capacitor, 0603, X7R	5-00764
C136	1000P	Capacitor, 0603, NPO	5-00740
C137	330P	Capacitor, 0603, NPO	5-00728
C138	330P	Capacitor, 0603, NPO	5-00728
C139	100P	Capacitor, 0603, NPO	5-00716
C140	330P	Capacitor, 0603, NPO	5-00728
C141	.047U	Capacitor, Metal Film	5-00054
C142	100000P	Capacitor, 0603, X7R	5-00764
C143	100000P	Capacitor, 0603, X7R	5-00764
C144	1000P	Capacitor, 0603, NPO	5-00740
C200	100000P	Capacitor, 0603, X7R	5-00764
C201	100000P	Capacitor, 0603, X7R	5-00764
C202	100000P	Capacitor, 0603, X7R	5-00764
C203	100000P	Capacitor, 0603, X7R	5-00764
C204	10000P	Capacitor, 0603, X7R	5-00752

C205	100000P	Capacitor, 0603, X7R	5-00764
C206	10000P	Capacitor, 0603, X7R	5-00752
C207	100000P	Capacitor, 0603, X7R	5-00764
C208	10000P	Capacitor, 0603, X7R	5-00752
C209	10000P	Capacitor, 0603, X7R	5-00752
C210	10000P	Capacitor, 0603, X7R	5-00752
C211	10000P	Capacitor, 0603, X7R	5-00752
C212	47P	Capacitor, 0603, NPO	5-00708
C213	47P	Capacitor, 0603, NPO	5-00708
C214	47P	Capacitor, 0603, NPO	5-00708
C215	10000P	Capacitor, 0603, X7R	5-00752
C216	22000P	Capacitor, 0603, X7R	5-00756
C217	10000P	Capacitor, 0603, X7R	5-00752
C218	220P	Capacitor, 0603, NPO	5-00724
C219	470P	Capacitor, 0603, NPO	5-00732
C220	220P	Capacitor, 0603, NPO	5-00724
C221	100000P	Capacitor, 0603, X7R	5-00764
C222	100000P	Capacitor, 0603, X7R	5-00764
C223	100000P	Capacitor, 0603, X7R	5-00764
C224	100000P	Capacitor, 0603, X7R	5-00764
C225	100000P	Capacitor, 0603, X7R	5-00764
C226	100000P	Capacitor, 0603, X7R	5-00764
C227	1000P	Capacitor, 0603, NPO	5-00740
C228	1000P	Capacitor, 0603, NPO	5-00740
C229	1000P	Capacitor, 0603, NPO	5-00740
C230	100000P	Capacitor, 0603, X7R	5-00764
C231	100000P	Capacitor, 0603, X7R	5-00764
C232	100000P	Capacitor, 0603, X7R	5-00764
C233	100000P	Capacitor, 0603, X7R	5-00764
C234	.47U / 16V	Capacitor, 1206, X7R	5-00527
C235	.47U / 16V	Capacitor, 1206, X7R	5-00527
C236	100000P	Capacitor, 0603, X7R	5-00764
C237	.01U	Capacitor, Metal Film	5-00052
C238	10UF / 6.3V	Ceramic, 16V, X5R	5-00657
C239	100000P	Capacitor, 0603, X7R	5-00764
C240	100000P	Capacitor, 0603, X7R	5-00764
C241	100000P	Capacitor, 0603, X7R	5-00764
C242	100000P	Capacitor, 0603, X7R	5-00764
C243	100000P	Capacitor, 0603, X7R	5-00764
C244	100000P	Capacitor, 0603, X7R	5-00764
C245	100000P	Capacitor, 0603, X7R	5-00764
C246	10UF / 6.3V	Ceramic, 16V, X5R	5-00657
C247	.39U - PP	Capacitor, Polypropylene, Radial	5-00837
C248	100P	Capacitor, 0603, NPO	5-00716
C249	.01U	Capacitor, Metal Film	5-00052
C250	56P	Capacitor, 0603, NPO	5-00710
C251	.01U	Capacitor, Metal Film	5-00052
C252	220P	Capacitor, 0603, NPO	5-00724
C253	220P	Capacitor, 0603, NPO	5-00724
C254	120P	Capacitor, 0603, NPO	5-00718
C255	56P	Capacitor, 0603, NPO	5-00710
C256	.39U - PP	Capacitor, Polypropylene, Radial	5-00837
C258	.047U	Capacitor, Metal Film	5-00054
C259	.047U	Capacitor, Metal Film	5-00054
C260	100000P	Capacitor, 0603, X7R	5-00764
C261	100000P	Capacitor, 0603, X7R	5-00764
C300	.22U / 16V	Capacitor	5-00836
C301	100000P	Capacitor, 0603, X7R	5-00764
C302	100000P	Capacitor, 0603, X7R	5-00764
C303	.22U / 16V	Capacitor	5-00836
C304	.22U / 16V	Capacitor	5-00836
C305	.22U / 16V	Capacitor	5-00836
C306	.22U / 16V	Capacitor	5-00836
C307	.22U / 16V	Capacitor	5-00836
C308	4.7UF / 50V X5R	Ceramic, 16V, X5R	5-00807
C309	100000P	Capacitor, 0603, X7R	5-00764
C310	.22U / 16V	Capacitor	5-00836
C311	100000P	Capacitor, 0603, X7R	5-00764
C312	.22U / 16V	Capacitor	5-00836
C313	100P	Capacitor, 0603, NPO	5-00716
C314	100000P	Capacitor, 0603, X7R	5-00764
C315	100000P	Capacitor, 0603, X7R	5-00764
C316	100000P	Capacitor, 0603, X7R	5-00764
C317	4.7UF / 50V X5R	Ceramic, 16V, X5R	5-00807
C318	100000P	Capacitor, 0603, X7R	5-00764
C319	100000P	Capacitor, 0603, X7R	5-00764
C320	100000P	Capacitor, 0603, X7R	5-00764
C321	100000P	Capacitor, 0603, X7R	5-00764
C323	100000P	Capacitor, 0603, X7R	5-00764
C324	100000P	Capacitor, 0603, X7R	5-00764
C325	100000P	Capacitor, 0603, X7R	5-00764
C326	100000P	Capacitor, 0603, X7R	5-00764
C327	100000P	Capacitor, 0603, X7R	5-00764
C328	100000P	Capacitor, 0603, X7R	5-00764
C329	100000P	Capacitor, 0603, X7R	5-00764
C330	100000P	Capacitor, 0603, X7R	5-00764
C331	100000P	Capacitor, 0603, X7R	5-00764
C332	10000P	Capacitor, 0603, X7R	5-00752
C333	100000P	Capacitor, 0603, X7R	5-00764
C334	100000P	Capacitor, 0603, X7R	5-00764
C335	100000P	Capacitor, 0603, X7R	5-00764
C336	100P	Capacitor, 0603, NPO	5-00716
C337	100P	Capacitor, 0603, NPO	5-00716
C400	100000P	Capacitor, 0603, X7R	5-00764
C401	100000P	Capacitor, 0603, X7R	5-00764
C402	10000P	Capacitor, 0603, X7R	5-00752
C403	10000P	Capacitor, 0603, X7R	5-00752
C404	10000P	Capacitor, 0603, X7R	5-00752
C406	10000P	Capacitor, 0603, X7R	5-00752
C407	10000P	Capacitor, 0603, X7R	5-00752
C409	10000P	Capacitor, 0603, X7R	5-00752
C410	10000P	Capacitor, 0603, X7R	5-00752
C412	10000P	Capacitor, 0603, X7R	5-00752
C413	10000P	Capacitor, 0603, X7R	5-00752
C414	10000P	Capacitor, 0603, X7R	5-00752
C415	100000P	Capacitor, 0603, X7R	5-00764
C416	100000P	Capacitor, 0603, X7R	5-00764
C417	10000P	Capacitor, 0603, X7R	5-00752
C419	10000P	Capacitor, 0603, X7R	5-00752
C420	10000P	Capacitor, 0603, X7R	5-00752
C421	10000P	Capacitor, 0603, X7R	5-00752
C422	10000P	Capacitor, 0603, X7R	5-00752
C424	10000P	Capacitor, 0603, X7R	5-00752
C427	10000P	Capacitor, 0603, X7R	5-00752
C429	10000P	Capacitor, 0603, X7R	5-00752
C430	10000P	Capacitor, 0603, X7R	5-00752
C431	10000P	Capacitor, 0603, X7R	5-00752
C432	10000P	Capacitor, 0603, X7R	5-00752
C433	10000P	Capacitor, 0603, X7R	5-00752
C434	10000P	Capacitor, 0603, X7R	5-00752
C437	100000P	Capacitor, 0603, X7R	5-00764
C438	100000P	Capacitor, 0603, X7R	5-00764
C439	100000P	Capacitor, 0603, X7R	5-00764
C440	100000P	Capacitor, 0603, X7R	5-00764
C500	100000P	Capacitor, 0603, X7R	5-00764
C501	100000P	Capacitor, 0603, X7R	5-00764
C502	100000P	Capacitor, 0603, X7R	5-00764
C503	100000P	Capacitor, 0603, X7R	5-00764
C504	100000P	Capacitor, 0603, X7R	5-00764
C505	2.2UF 16V /0603	Ceramic, 16V, X5R	5-00656
C506	100000P	Capacitor, 0603, X7R	5-00764
C507	2.7P	Capacitor, 0603, NPO	5-00677
C508	100000P	Capacitor, 0603, X7R	5-00764
C509	18P	Capacitor, 0603, NPO	5-00698
C510	.39U - PP	Capacitor, Polypropylene, Radial	5-00837
C511	100P	Capacitor, 0603, NPO	5-00716
C512	330P	Capacitor, 0603, NPO	5-00728
C513	1000P	Capacitor, 0603, NPO	5-00740
C514	330P	Capacitor, 0603, NPO	5-00728
C515	2.2UF 16V /0603	Ceramic, 16V, X5R	5-00656
C516	100000P	Capacitor, 0603, X7R	5-00764
C517	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C518	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C519	100000P	Capacitor, 0603, X7R	5-00764
C520	100000P	Capacitor, 0603, X7R	5-00764
C521	100000P	Capacitor, 0603, X7R	5-00764
C522	100000P	Capacitor, 0603, X7R	5-00764
C523	100P	Capacitor, 0603, NPO	5-00716
C524	680P	Capacitor, 0603, NPO	5-00736
C525	100000P	Capacitor, 0603, X7R	5-00764
C526	100000P	Capacitor, 0603, X7R	5-00764
C527	100000P	Capacitor, 0603, X7R	5-00764
C528	100000P	Capacitor, 0603, X7R	5-00764
C529	100P	Capacitor, 0603, NPO	5-00716
C530	680P	Capacitor, 0603, NPO	5-00736
C531	100000P	Capacitor, 0603, X7R	5-00764

C532	100P	Capacitor, 0603, NPO	5-00716
C533	680P	Capacitor, 0603, NPO	5-00736
C534	100000P	Capacitor, 0603, X7R	5-00764
C535	100000P	Capacitor, 0603, X7R	5-00764
C536	100P	Capacitor, 0603, NPO	5-00716
C537	680P	Capacitor, 0603, NPO	5-00736
C538	100000P	Capacitor, 0603, X7R	5-00764
C539	100000P	Capacitor, 0603, X7R	5-00764
C540	100P	Capacitor, 0603, NPO	5-00716
C541	680P	Capacitor, 0603, NPO	5-00736
C542	100000P	Capacitor, 0603, X7R	5-00764
C543	100000P	Capacitor, 0603, X7R	5-00764
C544	100000P	Capacitor, 0603, X7R	5-00764
C545	100P	Capacitor, 0603, NPO	5-00716
C546	680P	Capacitor, 0603, NPO	5-00736
C547	100000P	Capacitor, 0603, X7R	5-00764
C548	100000P	Capacitor, 0603, X7R	5-00764
C549	100000P	Capacitor, 0603, X7R	5-00764
C550	100000P	Capacitor, 0603, X7R	5-00764
C551	100P	Capacitor, 0603, NPO	5-00716
C552	680P	Capacitor, 0603, NPO	5-00736
C553	100000P	Capacitor, 0603, X7R	5-00764
C554	100000P	Capacitor, 0603, X7R	5-00764
C555	100P	Capacitor, 0603, NPO	5-00716
C556	680P	Capacitor, 0603, NPO	5-00736
C557	100000P	Capacitor, 0603, X7R	5-00764
C558	100000P	Capacitor, 0603, X7R	5-00764
C559	100000P	Capacitor, 0603, X7R	5-00764
C560	100000P	Capacitor, 0603, X7R	5-00764
C600	100000P	Capacitor, 0603, X7R	5-00764
C601	100000P	Capacitor, 0603, X7R	5-00764
C602	1000P	Capacitor, 0603, NPO	5-00740
C603	4.7UF / 50V X5R	Ceramic, 16V, X5R	5-00807
C604	4.7UF / 50V X5R	Ceramic, 16V, X5R	5-00807
C605	10000P	Capacitor, 0603, X7R	5-00752
C606	10000P	Capacitor, 0603, X7R	5-00752
C607	100000P	Capacitor, 0603, X7R	5-00764
C608	10UF / 6.3V	Ceramic, 16V, X5R	5-00657
C609	100000P	Capacitor, 0603, X7R	5-00764
C610	100000P	Capacitor, 0603, X7R	5-00764
C611	100000P	Capacitor, 0603, X7R	5-00764
C612	100000P	Capacitor, 0603, X7R	5-00764
C613	100000P	Capacitor, 0603, X7R	5-00764
C614	100000P	Capacitor, 0603, X7R	5-00764
C615	100000P	Capacitor, 0603, X7R	5-00764
C616	10UF / 6.3V	Ceramic, 16V, X5R	5-00657
C617	100000P	Capacitor, 0603, X7R	5-00764
C619	.047U	Capacitor, Metal Film	5-00054
C620	4.7UF / 50V X5R	Ceramic, 16V, X5R	5-00807
C621	10UF / 6.3V	Ceramic, 16V, X5R	5-00657
C622	100000P	Capacitor, 0603, X7R	5-00764
C623	100000P	Capacitor, 0603, X7R	5-00764
C624	100000P	Capacitor, 0603, X7R	5-00764
C625	100000P	Capacitor, 0603, X7R	5-00764
C626	100000P	Capacitor, 0603, X7R	5-00764
C627	100000P	Capacitor, 0603, X7R	5-00764
C628	100000P	Capacitor, 0603, X7R	5-00764
C629	10UF / 6.3V	Ceramic, 16V, X5R	5-00657
C630	100000P	Capacitor, 0603, X7R	5-00764
C631	100P	Capacitor, 0603, NPO	5-00716
C632	100000P	Capacitor, 0603, X7R	5-00764
C633	.39U - PP	Capacitor, Polypropylene, Radial	5-00837
C634	.01U	Capacitor, Metal Film	5-00052
C635	.01U	Capacitor, Metal Film	5-00052
C636	10P	Capacitor, 0603, NPO	5-00692
C637	.0033U	Capacitor, Polyester Film	5-00050
C638	10P	Capacitor, 0603, NPO	5-00692
C639	100P	Capacitor, 0603, NPO	5-00716
C640	100P	Capacitor, 0603, NPO	5-00716
C641	4.7UF / 50V X5R	Ceramic, 16V, X5R	5-00807
C700	100000P	Capacitor, 0603, X7R	5-00764
C701	100000P	Capacitor, 0603, X7R	5-00764
C702	100000P	Capacitor, 0603, X7R	5-00764
C703	100000P	Capacitor, 0603, X7R	5-00764
C704	100000P	Capacitor, 0603, X7R	5-00764
C705	100000P	Capacitor, 0603, X7R	5-00764
C706	100000P	Capacitor, 0603, X7R	5-00764
C707	2.7P	Capacitor, 0603, NPO	5-00677
C708	18P	Capacitor, 0603, NPO	5-00698
C709	7.5P	Capacitor, 0603, NPO	5-00689
C710	100000P	Capacitor, 0603, X7R	5-00764
C711	2.7P	Capacitor, 0603, NPO	5-00677
C712	18P	Capacitor, 0603, NPO	5-00698
C713	7.5P	Capacitor, 0603, NPO	5-00689
C714	100000P	Capacitor, 0603, X7R	5-00764
C715	100P	Capacitor, 0603, NPO	5-00716
C716	100000P	Capacitor, 0603, X7R	5-00764
C717	100000P	Capacitor, 0603, X7R	5-00764
C718	100000P	Capacitor, 0603, X7R	5-00764
C719	100000P	Capacitor, 0603, X7R	5-00764
C720	100000P	Capacitor, 0603, X7R	5-00764
C721	100000P	Capacitor, 0603, X7R	5-00764
C722	100000P	Capacitor, 0603, X7R	5-00764
C723	100000P	Capacitor, 0603, X7R	5-00764
C724	100000P	Capacitor, 0603, X7R	5-00764
C725	100000P	Capacitor, 0603, X7R	5-00764
C726	100000P	Capacitor, 0603, X7R	5-00764
C727	100000P	Capacitor, 0603, X7R	5-00764
C800	4.7UF / 50V X5R	Ceramic, 16V, X5R	5-00807
C801	1000P	Capacitor, 0603, NPO	5-00740
C802	4.7UF / 50V X5R	Ceramic, 16V, X5R	5-00807
C803	100000P	Capacitor, 0603, X7R	5-00764
C804	4.7UF / 50V X5R	Ceramic, 16V, X5R	5-00807
C805	100000P	Capacitor, 0603, X7R	5-00764
C806	4.7UF / 50V X5R	Ceramic, 16V, X5R	5-00807
C807	10000P	Capacitor, 0603, X7R	5-00752
C808	4.7UF / 50V X5R	Ceramic, 16V, X5R	5-00807
C809	100000P	Capacitor, 0603, X7R	5-00764
C810	4.7UF / 50V X5R	Ceramic, 16V, X5R	5-00807
C811	100000P	Capacitor, 0603, X7R	5-00764
C812	4.7UF / 50V X5R	Ceramic, 16V, X5R	5-00807
C813	100000P	Capacitor, 0603, X7R	5-00764
C814	10UF / 6.3V	Ceramic, 16V, X5R	5-00657
C815	100000P	Capacitor, 0603, X7R	5-00764
C816	4.7UF / 50V X5R	Ceramic, 16V, X5R	5-00807
C817	100000P	Capacitor, 0603, X7R	5-00764
C818	1000P	Capacitor, 0603, NPO	5-00740
C819	100000P	Capacitor, 0603, X7R	5-00764
C820	10UF / 6.3V	Ceramic, 16V, X5R	5-00657
C821	100000P	Capacitor, 0603, X7R	5-00764
C822	2200P	Capacitor, 0603, X7R	5-00744
C823	100000P	Capacitor, 0603, X7R	5-00764
C824	100000P	Capacitor, 0603, X7R	5-00764
C825	10UF / 6.3V	Ceramic, 16V, X5R	5-00657
C826	100000P	Capacitor, 0603, X7R	5-00764
C827	4.7UF / 50V X5R	Ceramic, 16V, X5R	5-00807
C828	100000P	Capacitor, 0603, X7R	5-00764
C829	10000P	Capacitor, 0603, X7R	5-00752
C830	100000P	Capacitor, 0603, X7R	5-00764
C831	10U/T16	SMD TANTALUM, C-Case	5-00471
C832	100000P	Capacitor, 0603, X7R	5-00764
C833	4.7UF / 50V X5R	Ceramic, 16V, X5R	5-00807
D100	MMBV609	DUAL VARACTOR	3-00803
D101	BAV99	Dual Series Diode	3-00896
D200	MMBV609	DUAL VARACTOR	3-00803
D201	MMBV609	DUAL VARACTOR	3-00803
D202	MMBV609	DUAL VARACTOR	3-00803
D500	MMBZ5222BLT1G	2.5V Zener	3-02013
D501	BAV99	Dual Series Diode	3-00896
D502	BAV99	Dual Series Diode	3-00896
D503	MMBZ5222BLT1G	2.5V Zener	3-02013
D504	BAV99	Dual Series Diode	3-00896
D800	RED	LED, T1 Package	3-00011
J100	26-48-1101	Connector	1-01057
J101	73100-0195	Panel Mount BNC	1-01158
J102	73100-0195	Panel Mount BNC	1-01158
J300	26 PIN	Connector	1-01178
J301	DEKL-9SAT-E	Connector	1-01031
J302	9 PIN	Connector	1-01247
J303	IEEE488/STAND.	Connector	1-00160
J400	TSW-106-08-G-S	Connector	1-01146
J500	73100-0195	Panel Mount BNC	1-01158
J501	73100-0195	Panel Mount BNC	1-01158
J700	34 PIN	Connector	1-01256
J701	25 PIN	Connector	1-01255
J702	43860-0001	Connector	1-01380

J800	10M156(LONG)	Connector	1-00555
L100	22UH -SMT	Fixed inductor	6-00659
L101	2506031517Y0	Inductor BEAD 0603	6-00759
L102	2A / 1806	BEAD SMD 1806	6-00744
L103	.68UH	Fixed inductor	6-00988
L104	2506031517Y0	Inductor BEAD 0603	6-00759
L105	6.8UH - 1210	Fixed inductor	6-00667
L106	2506031517Y0	Inductor BEAD 0603	6-00759
L107	6.8UH - 1210	Fixed inductor	6-00667
L108	2506031517Y0	Inductor BEAD 0603	6-00759
L109	2506031517Y0	Inductor BEAD 0603	6-00759
L110	2506031517Y0	Inductor BEAD 0603	6-00759
L111	.68UH	Fixed inductor	6-00988
L112	2506031517Y0	Inductor BEAD 0603	6-00759
L200	22UH -SMT	Fixed inductor	6-00659
L201	22UH -SMT	Fixed inductor	6-00659
L202	22UH -SMT	Fixed inductor	6-00659
L203	6.8UH - 1210	Fixed inductor	6-00667
L204	6.8UH - 1210	Fixed inductor	6-00667
L205	6.8UH - 1210	Fixed inductor	6-00667
L206	22UH -SMT	Fixed inductor	6-00659
L207	.68UH	Fixed inductor	6-00988
L208	22UH -SMT	Fixed inductor	6-00659
L209	2506031517Y0	Inductor BEAD 0603	6-00759
L210	2506031517Y0	Inductor BEAD 0603	6-00759
L211	2506031517Y0	Inductor BEAD 0603	6-00759
L212	2506031517Y0	Inductor BEAD 0603	6-00759
L213	2506031517Y0	Inductor BEAD 0603	6-00759
L214	2506031517Y0	Inductor BEAD 0603	6-00759
L215	2506031517Y0	Inductor BEAD 0603	6-00759
L216	2506031517Y0	Inductor BEAD 0603	6-00759
L217	0.33uH	Fixed inductor	6-01011
L218	0.33uH	Fixed inductor	6-01011
L219	0.33uH	Fixed inductor	6-01011
L220	0.33uH	Fixed inductor	6-01011
L221	0.33uH	Fixed inductor	6-01011
L222	0.33uH	Fixed inductor	6-01011
L300	2506031517Y0	Inductor BEAD 0603	6-00759
L301	2506031517Y0	Inductor BEAD 0603	6-00759
L302	2506031517Y0	Inductor BEAD 0603	6-00759
L303	2506031517Y0	Inductor BEAD 0603	6-00759
L304	2506031517Y0	Inductor BEAD 0603	6-00759
L305	2506031517Y0	Inductor BEAD 0603	6-00759
L307	2506031517Y0	Inductor BEAD 0603	6-00759
L308	2506031517Y0	Inductor BEAD 0603	6-00759
L309	2506031517Y0	Inductor BEAD 0603	6-00759
L310	2506031517Y0	Inductor BEAD 0603	6-00759
L400	2506031517Y0	Inductor BEAD 0603	6-00759
L402	2506031517Y0	Inductor BEAD 0603	6-00759
L403	2506031517Y0	Inductor BEAD 0603	6-00759
L404	2506031517Y0	Inductor BEAD 0603	6-00759
L405	2506031517Y0	Inductor BEAD 0603	6-00759
L406	2506031517Y0	Inductor BEAD 0603	6-00759
L407	2506031517Y0	Inductor BEAD 0603	6-00759
L408	2506031517Y0	Inductor BEAD 0603	6-00759
L409	47NH	Fixed inductor	6-01000
L500	2506031517Y0	Inductor BEAD 0603	6-00759
L501	2506031517Y0	Inductor BEAD 0603	6-00759
L502	2506031517Y0	Inductor BEAD 0603	6-00759
L503	10UH	Fixed inductor	6-00684
L504	22UH -SMT	Fixed inductor	6-00659
L505	2506031517Y0	Inductor BEAD 0603	6-00759
L506	2506031517Y0	Inductor BEAD 0603	6-00759
L507	2506031517Y0	Inductor BEAD 0603	6-00759
L508	2506031517Y0	Inductor BEAD 0603	6-00759
L509	.68UH	Fixed inductor	6-00988
L510	.68UH	Fixed inductor	6-00988
L511	2506031517Y0	Inductor BEAD 0603	6-00759
L512	2506031517Y0	Inductor BEAD 0603	6-00759
L513	.68UH	Fixed inductor	6-00988
L514	.68UH	Fixed inductor	6-00988
L515	2506031517Y0	Inductor BEAD 0603	6-00759
L516	2506031517Y0	Inductor BEAD 0603	6-00759
L517	2506031517Y0	Inductor BEAD 0603	6-00759
L518	2506031517Y0	Inductor BEAD 0603	6-00759
L519	.68UH	Fixed inductor	6-00988
L520	.68UH	Fixed inductor	6-00988
L521	2506031517Y0	Inductor BEAD 0603	6-00759
L522	2506031517Y0	Inductor BEAD 0603	6-00759
L523	.68UH	Fixed inductor	6-00988
L524	.68UH	Fixed inductor	6-00988
L525	2506031517Y0	Inductor BEAD 0603	6-00759
L600	2506031517Y0	Inductor BEAD 0603	6-00759
L601	2506031517Y0	Inductor BEAD 0603	6-00759
L602	2506031517Y0	Inductor BEAD 0603	6-00759
L604	2506031517Y0	Inductor BEAD 0603	6-00759
L605	2506031517Y0	Inductor BEAD 0603	6-00759
L606	2506031517Y0	Inductor BEAD 0603	6-00759
L607	150NH	Fixed inductor	6-00989
L608	150NH	Fixed inductor	6-00989
L700	150NH	Fixed inductor	6-00989
L701	150NH	Fixed inductor	6-00989
L702	2506031517Y0	Inductor BEAD 0603	6-00759
L703	2506031517Y0	Inductor BEAD 0603	6-00759
L704	2506031517Y0	Inductor BEAD 0603	6-00759
L705	2506031517Y0	Inductor BEAD 0603	6-00759
L706	150NH	Fixed inductor	6-00989
L707	150NH	Fixed inductor	6-00989
L708	2506031517Y0	Inductor BEAD 0603	6-00759
L709	2506031517Y0	Inductor BEAD 0603	6-00759
L710	2506031517Y0	Inductor BEAD 0603	6-00759
L711	2506031517Y0	Inductor BEAD 0603	6-00759
L712	2506031517Y0	Inductor BEAD 0603	6-00759
L800	2A / 1806	BEAD SMD 1806	6-00744
L801	2A / 1806	BEAD SMD 1806	6-00744
L802	2A / 1806	BEAD SMD 1806	6-00744
L803	2A / 1806	BEAD SMD 1806	6-00744
L804	2A / 1806	BEAD SMD 1806	6-00744
L805	2A / 1806	BEAD SMD 1806	6-00744
L806	2A / 1806	BEAD SMD 1806	6-00744
L807	2A / 1806	BEAD SMD 1806	6-00744
L808	2506031517Y0	Inductor BEAD 0603	6-00759
PC1	SG385 M/B	Fabricated component	7-02098
Q100	MMBT5179	NPN Transistor	3-00808
Q101	MMBTH81LT1	UHF PNP Transistor	3-00809
Q200	MMBT5179	NPN Transistor	3-00808
Q201	MMBT5179	NPN Transistor	3-00808
Q202	MMBT5179	NPN Transistor	3-00808
Q203	MMBTH81LT1	UHF PNP Transistor	3-00809
Q204	MMBTH81LT1	UHF PNP Transistor	3-00809
Q205	MMBTH81LT1	UHF PNP Transistor	3-00809
Q500	MMBT3904LT1	NPN Transistor	3-00601
Q800	MMBT5179	NPN Transistor	3-00808
R100	1.00K	Resistor, 0603, Thin Film	4-02157
R101	4.99K	Resistor, 0603, Thin Film	4-02224
R102	1.00K	Resistor, 0603, Thin Film	4-02157
R103	1.00K	Resistor, 0603, Thin Film	4-02157
R104	10.0K	Resistor, 0603, Thin Film	4-02253
R105	1.00K	Resistor, 0603, Thin Film	4-02157
R106	100	Resistor, 0603, Thin Film	4-02061
R107	30.1	Resistor, 0603, Thin Film	4-02011
R108	100K	Resistor, 0603, Thin Film	4-02349
R109	1.00K	Resistor, 0603, Thin Film	4-02157
R110	10	Resistor, 0603, Thin Film	4-01965
R111	100K	Resistor, 0603, Thin Film	4-02349
R112	10.0K	Resistor, 0603, Thin Film	4-02253
R113	10	Resistor, 0603, Thin Film	4-01965
R114	24.9	Resistor, 0603, Thin Film	4-02003
R115	1.00K	Resistor, 0603, Thin Film	4-02157
R116	10.0K	Resistor, 0603, Thin Film	4-02253
R117	1.00K	Resistor, 0603, Thin Film	4-02157
R118	10.0K	Resistor, 0603, Thin Film	4-02253
R119	1.00K	Resistor, 0603, Thin Film	4-02157
R120	10.0K	Resistor, 0603, Thin Film	4-02253
R121	200	Resistor, 0603, Thin Film	4-02090
R122	249	Resistor, 0603, Thin Film	4-02099
R123	499	Resistor, 0603, Thin Film	4-02128
R124	30.1	Resistor, 0603, Thin Film	4-02011
R125	4.99K	Resistor, 0603, Thin Film	4-02224
R126	10.0K	Resistor, 0603, Thin Film	4-02253
R127	10.0K	Resistor, 0603, Thin Film	4-02253
R128	49.9K	Resistor, 0603, Thin Film	4-02320
R129	49.9K	Resistor, 0603, Thin Film	4-02320
R130	100	Resistor, 0603, Thin Film	4-02061
R131	49.9K	Resistor, 0603, Thin Film	4-02320
R132	10.0K	Resistor, 0603, Thin Film	4-02253

R133	10.0K	Resistor, 0603, Thin Film	4-02253
R134	10.0K	Resistor, 0603, Thin Film	4-02253
R135	100	Resistor, 0603, Thin Film	4-02061
R136	100	Resistor, 0603, Thin Film	4-02061
R137	10.0K	Resistor, 0603, Thin Film	4-02253
R138	100	Resistor, 0603, Thin Film	4-02061
R139	1.00K	Resistor, 0603, Thin Film	4-02157
R140	10.0K	Resistor, 0603, Thin Film	4-02253
R141	4.99K	Resistor, 0603, Thin Film	4-02224
R142	10.0K	Resistor, 0603, Thin Film	4-02253
R143	30.1	Resistor, 0603, Thin Film	4-02011
R144	30.1	Resistor, 0603, Thin Film	4-02011
R145	100	Resistor, 0603, Thin Film	4-02061
R146	100	Resistor, 0603, Thin Film	4-02061
R147	49.9	Resistor, 0603, Thin Film	4-02032
R148	49.9	Resistor, 0603, Thin Film	4-02032
R149	24.9	Resistor, 0603, Thin Film	4-02003
R150	24.9	Resistor, 0603, Thin Film	4-02003
R200	4.99K	Resistor, 0603, Thin Film	4-02224
R201	1.00K	Resistor, 0603, Thin Film	4-02157
R202	2.00K	Resistor, 0603, Thin Film	4-02186
R203	1.00K	Resistor, 0603, Thin Film	4-02157
R204	4.99K	Resistor, 0603, Thin Film	4-02224
R205	1.00K	Resistor, 0603, Thin Film	4-02157
R206	10.0K	Resistor, 0603, Thin Film	4-02253
R207	10.0K	Resistor, 0603, Thin Film	4-02253
R208	10.0K	Resistor, 0603, Thin Film	4-02253
R209	100	Resistor, 0603, Thin Film	4-02061
R210	100	Resistor, 0603, Thin Film	4-02061
R211	100	Resistor, 0603, Thin Film	4-02061
R212	1.00K	Resistor, 0603, Thin Film	4-02157
R213	1.00K	Resistor, 0603, Thin Film	4-02157
R214	1.00K	Resistor, 0603, Thin Film	4-02157
R215	10.0K	Resistor, 0603, Thin Film	4-02253
R216	10.0K	Resistor, 0603, Thin Film	4-02253
R217	10.0K	Resistor, 0603, Thin Film	4-02253
R218	100K	Resistor, 0603, Thin Film	4-02349
R219	1.00K	Resistor, 0603, Thin Film	4-02157
R220	100K	Resistor, 0603, Thin Film	4-02349
R221	1.00K	Resistor, 0603, Thin Film	4-02157
R222	100K	Resistor, 0603, Thin Film	4-02349
R223	1.00K	Resistor, 0603, Thin Film	4-02157
R224	10	Resistor, 0603, Thin Film	4-01965
R225	10	Resistor, 0603, Thin Film	4-01965
R226	10	Resistor, 0603, Thin Film	4-01965
R227	100K	Resistor, 0603, Thin Film	4-02349
R228	100K	Resistor, 0603, Thin Film	4-02349
R229	100K	Resistor, 0603, Thin Film	4-02349
R230	24.9	Resistor, 0603, Thin Film	4-02003
R231	10	Resistor, 0603, Thin Film	4-01965
R232	24.9	Resistor, 0603, Thin Film	4-02003
R233	24.9	Resistor, 0603, Thin Film	4-02003
R234	24.9	Resistor, 0603, Thin Film	4-02003
R235	24.9	Resistor, 0603, Thin Film	4-02003
R236	10.0K	Resistor, 0603, Thin Film	4-02253
R237	10.0K	Resistor, 0603, Thin Film	4-02253
R238	10.0K	Resistor, 0603, Thin Film	4-02253
R239	1.00K	Resistor, 0603, Thin Film	4-02157
R240	1.00K	Resistor, 0603, Thin Film	4-02157
R241	1.00K	Resistor, 0603, Thin Film	4-02157
R242	45.3	Resistor, 0603, Thin Film	4-02028
R243	45.3	Resistor, 0603, Thin Film	4-02028
R244	45.3	Resistor, 0603, Thin Film	4-02028
R245	249	Resistor, 0603, Thin Film	4-02099
R246	499	Resistor, 0603, Thin Film	4-02128
R247	249	Resistor, 0603, Thin Film	4-02099
R248	499	Resistor, 0603, Thin Film	4-02128
R249	249	Resistor, 0603, Thin Film	4-02099
R250	499	Resistor, 0603, Thin Film	4-02128
R251	10.0K	Resistor, 0603, Thin Film	4-02253
R252	100K	Resistor, 0603, Thin Film	4-02349
R253	20.0K	Resistor, 0603, Thin Film	4-02282
R254	10.0K	Resistor, 0603, Thin Film	4-02253
R255	2.80K	Resistor, 0603, Thin Film	4-02200
R256	1.00K	Resistor, 0603, Thin Film	4-02157
R257	200	Resistor, 0603, Thin Film	4-02090
R258	49.9K	Resistor, 0603, Thin Film	4-02320
R259	200	Resistor, 0603, Thin Film	4-02090
R260	10.0K	Resistor, 0603, Thin Film	4-02253
R261	100	Resistor, 0603, Thin Film	4-02061
R262	200	Resistor, 0603, Thin Film	4-02090
R263	4.99K	Resistor, 0603, Thin Film	4-02224
R264	4.99K	Resistor, 0603, Thin Film	4-02224
R265	200	Resistor, 0603, Thin Film	4-02090
R266	4.02K	Resistor, 0603, Thin Film	4-02215
R267	100K	Resistor, 0603, Thin Film	4-02349
R268	49.9K	Resistor, 0603, Thin Film	4-02320
R269	10.0K	Resistor, 0603, Thin Film	4-02253
R270	20.0K	Resistor, 0603, Thin Film	4-02282
R271	10.0K	Resistor, 0603, Thin Film	4-02253
R272	49.9	Resistor, 0603, Thin Film	4-02032
R273	49.9	Resistor, 0603, Thin Film	4-02032
R300	12.1K	Resistor, 0603, Thin Film	4-02261
R301	100	Resistor, 0603, Thin Film	4-02061
R302	100	Resistor, 0603, Thin Film	4-02061
R303	1.00K	Resistor, 0603, Thin Film	4-02157
R304	100	Resistor, 0603, Thin Film	4-02061
R305	100K	Resistor, 0603, Thin Film	4-02349
R306	10.0K	Resistor, 0603, Thin Film	4-02253
R307	10.0K	Resistor, 0603, Thin Film	4-02253
R308	10.0K	Resistor, 0603, Thin Film	4-02253
R309	49.9	Resistor, 0603, Thin Film	4-02032
R310	49.9	Resistor, 0603, Thin Film	4-02032
R311	10.0K	Resistor, 0603, Thin Film	4-02253
R312	100	Resistor, 0603, Thin Film	4-02061
R313	100	Resistor, 0603, Thin Film	4-02061
R314	100	Resistor, 0603, Thin Film	4-02061
R400	49.9	Resistor, 0603, Thin Film	4-02032
R500	10.0K	Resistor, 0603, Thin Film	4-02253
R501	1.00K	Resistor, 0603, Thin Film	4-02157
R502	49.9K	Resistor, 0603, Thin Film	4-02320
R503	10.0K	Resistor, 0603, Thin Film	4-02253
R504	100	Resistor, 0603, Thin Film	4-02061
R505	49.9K	Resistor, 0603, Thin Film	4-02320
R506	49.9	Resistor, 0603, Thin Film	4-02032
R507	49.9K	Resistor, 0603, Thin Film	4-02320
R508	200	Resistor, 0603, Thin Film	4-02090
R509	49.9	Resistor, 0603, Thin Film	4-02032
R510	100K	Resistor, 0603, Thin Film	4-02349
R511	249	Resistor, 0603, Thin Film	4-02099
R512	100	Resistor, 0603, Thin Film	4-02061
R513	100	Resistor, 0603, Thin Film	4-02061
R514	49.9	Resistor, 0603, Thin Film	4-02032
R515	49.9	Resistor, 0603, Thin Film	4-02032
R516	49.9	Resistor, 0603, Thin Film	4-02032
R517	53.6	Resistor, 0603, Thin Film	4-02035
R518	49.9	Resistor, 0603, Thin Film	4-02032
R519	499	Resistor, 0603, Thin Film	4-02128
R520	402	Resistor, 0603, Thin Film	4-02119
R521	49.9	Resistor, 0603, Thin Film	4-02032
R522	53.6	Resistor, 0603, Thin Film	4-02035
R523	49.9	Resistor, 0603, Thin Film	4-02032
R524	49.9	Resistor, 0603, Thin Film	4-02032
R525	2.00K	Resistor, 0603, Thin Film	4-02186
R526	49.9	Resistor, 0603, Thin Film	4-02032
R527	49.9	Resistor, 0603, Thin Film	4-02032
R528	53.6	Resistor, 0603, Thin Film	4-02035
R529	49.9	Resistor, 0603, Thin Film	4-02032
R530	10KX4D	Resistor network	4-00912
R531	49.9	Resistor, 0603, Thin Film	4-02032
R532	53.6	Resistor, 0603, Thin Film	4-02035
R533	49.9	Resistor, 0603, Thin Film	4-02032
R534	53.6	Resistor, 0603, Thin Film	4-02035
R535	10.0K	Resistor, 0603, Thin Film	4-02253
R536	45.3	Resistor, 0603, Thin Film	4-02028
R537	45.3	Resistor, 0603, Thin Film	4-02028
R538	49.9	Resistor, 0603, Thin Film	4-02032
R539	53.6	Resistor, 0603, Thin Film	4-02035
R540	2.00K	Resistor, 0603, Thin Film	4-02186
R541	49.9	Resistor, 0603, Thin Film	4-02032
R542	53.6	Resistor, 0603, Thin Film	4-02035
R543	45.3	Resistor, 0603, Thin Film	4-02028
R544	45.3	Resistor, 0603, Thin Film	4-02028
R545	49.9	Resistor, 0603, Thin Film	4-02032
R546	53.6	Resistor, 0603, Thin Film	4-02035
R547	2.00K	Resistor, 0603, Thin Film	4-02186

R548	2.00K	Resistor, 0603, Thin Film	4-02186
R549	1.00K	Resistor, 0603, Thin Film	4-02157
R550	499	Resistor, 0603, Thin Film	4-02128
R551	100	Resistor, 0603, Thin Film	4-02061
R552	2.00K	Resistor, 0603, Thin Film	4-02186
R553	4.99K	Resistor, 0603, Thin Film	4-02224
R600	49.9	Resistor, 0603, Thin Film	4-02032
R601	49.9	Resistor, 0603, Thin Film	4-02032
R602	1.00K	Resistor, 0603, Thin Film	4-02157
R603	1.00K	Resistor, 0603, Thin Film	4-02157
R604	10.0K	Resistor, 0603, Thin Film	4-02253
R605	1.00K	Resistor, 0603, Thin Film	4-02157
R606	100	Resistor, 0603, Thin Film	4-02061
R607	10.0K	Resistor, 0603, Thin Film	4-02253
R608	30.1	Resistor, 0603, Thin Film	4-02011
R609	10.0K	Resistor, 0603, Thin Film	4-02253
R610	100	Resistor, 0603, Thin Film	4-02061
R611	1.00K	Resistor, 0603, Thin Film	4-02157
R612	100	Resistor, 0603, Thin Film	4-02061
R613	357	Resistor, 0603, Thin Film	4-02114
R614	20.0K	Resistor, 0603, Thin Film	4-02282
R615	1.00K	Resistor, 0603, Thin Film	4-02157
R616	100	Resistor, 0603, Thin Film	4-02061
R617	4.99K	Resistor, 0603, Thin Film	4-02224
R618	100	Resistor, 0603, Thin Film	4-02061
R619	49.9K	Resistor, 0603, Thin Film	4-02320
R620	20.0K	Resistor, 0603, Thin Film	4-02282
R621	10.0K	Resistor, 0603, Thin Film	4-02253
R700	100	Resistor, 0603, Thin Film	4-02061
R701	357	Resistor, 0603, Thin Film	4-02114
R702	4.99K	Resistor, 0603, Thin Film	4-02224
R703	100	Resistor, 0603, Thin Film	4-02061
R704	45.3	Resistor, 0603, Thin Film	4-02028
R705	100	Resistor, 0603, Thin Film	4-02061
R706	4.99K	Resistor, 0603, Thin Film	4-02224
R707	45.3	Resistor, 0603, Thin Film	4-02028
R708	715	Resistor, 0603, Thin Film	4-02143
R709	100	Resistor, 0603, Thin Film	4-02061
R710	357	Resistor, 0603, Thin Film	4-02114
R713	10.0K	Resistor, 0603, Thin Film	4-02253
R714	49.9	Resistor, 0603, Thin Film	4-02032
R715	49.9	Resistor, 0603, Thin Film	4-02032
R716	10.0K	Resistor, 0603, Thin Film	4-02253
R717	49.9	Resistor, 0603, Thin Film	4-02032
R718	49.9	Resistor, 0603, Thin Film	4-02032
R719	20.0K	Resistor, 0603, Thin Film	4-02282
R720	10.0K	Resistor, 0603, Thin Film	4-02253
R721	150K	Resistor, 0603, Thin Film	4-02366
R722	49.9K	Resistor, 0603, Thin Film	4-02320
R723	249	Resistor, 0603, Thin Film	4-02099
R724	249	Resistor, 0603, Thin Film	4-02099
R725	249	Resistor, 0603, Thin Film	4-02099
R726	249	Resistor, 0603, Thin Film	4-02099
R727	249	Resistor, 0603, Thin Film	4-02099
R728	249	Resistor, 0603, Thin Film	4-02099
R729	249	Resistor, 0603, Thin Film	4-02099
R730	249	Resistor, 0603, Thin Film	4-02099
R800	10.0K	Resistor, 0603, Thin Film	4-02253
R801	100K	Resistor, 0603, Thin Film	4-02349
R802	1.00K	Resistor, 0603, Thin Film	4-02157
R803	15.8K	Resistor, 0603, Thin Film	4-02272
R804	100K	Resistor, 0603, Thin Film	4-02349
R805	150K	Resistor, 0603, Thin Film	4-02366
R806	49.9K	Resistor, 0603, Thin Film	4-02320
R807	10.0K	Resistor, 0603, Thin Film	4-02253
R808	10.0K	Resistor, 0603, Thin Film	4-02253
R809	1.50K	Resistor, 0603, Thin Film	4-02174
R810	124	Resistor, 0603, Thin Film	4-02070
R811	1.00K	Resistor, 0603, Thin Film	4-02157
R812	715	Resistor, 0603, Thin Film	4-02143
R813	825	Resistor, 0603, Thin Film	4-02149
R814	1.00K	Resistor, 0603, Thin Film	4-02157
R815	200	Resistor, 0603, Thin Film	4-02090
R816	124	Resistor, 0603, Thin Film	4-02070
R817	1.00K	Resistor, 0603, Thin Film	4-02157
R818	715	Resistor, 0603, Thin Film	4-02143
RN100	10KX4D	Resistor network	4-00912
RN101	10KX4D	Resistor network	4-00912
RN103	8x150 OHM	Resistor network	4-02506
RN104	4x47 OHM	Resistor network	4-02505
RN300	100Kx4D 5%	Resistor network	4-01704
RN301	100Kx4D 5%	Resistor network	4-01704
RN302	4x47 OHM	Resistor network	4-02505
RN303	10KX4D	Resistor network	4-00912
RN304	10KX4D	Resistor network	4-00912
RN400	4x100 ohm	Resistor network	4-02503
RN500	1.0KX4D	Resistor network	4-00910
RN700	10KX4D	Resistor network	4-00912
SW800	DPDT	Switch	2-00023
T100	TC4-1T	Transformer	6-00767
T200	TC4-1T	Transformer	6-00767
U100	MMBD352L-ROHS	DUAL SCHOTTKY DIODE	3-00538
U101	LM321MF/NOPB	Single Op amp	3-02010
U102	LP5900SD-3.3	Low noise regulator	3-01784
U103	74LVC1G3157DBVR	SPDT Analog Switch	3-02015
U104	MMBD352L-ROHS	DUAL SCHOTTKY DIODE	3-00538
U105	MMBD352L-ROHS	DUAL SCHOTTKY DIODE	3-00538
U106	ADF4002BRUZ	RF PLL synthesizer	3-01755
U107	ADA4860-1YRJZ	Current FB Op-amp	3-02003
U108	74LVC1G3157DBVR	SPDT Analog Switch	3-02015
U109	74LVC1G3157DBVR	SPDT Analog Switch	3-02015
U110	ADTL082ARMZ	Dual Op amp	3-02006
U111	MMBD352L-ROHS	DUAL SCHOTTKY DIODE	3-00538
U112	LP5900SD-3.3	Low noise regulator	3-01784
U113	LP5900SD-3.3	Low noise regulator	3-01784
U114	74LVC1GX04DCKR	Crystal Driver	3-01998
U115	74LVC2G74DCTR	Single D-type flip flop	3-01867
U116	ADF4002BRUZ	RF PLL synthesizer	3-01755
U118	TLV2371IDBVR	Single R-R Op Amp	3-02016
U119	100.000MHZ	VCXO	6-00760
U120	74LVC2G74DCTR	Single D-type flip flop	3-01867
U121	74LVC2G74DCTR	Single D-type flip flop	3-01867
U122	65LVDS2DBV	LVDS Receiver	3-01770
U200	LM321MF/NOPB	Single Op amp	3-02010
U201	LM321MF/NOPB	Single Op amp	3-02010
U202	LM321MF/NOPB	Single Op amp	3-02010
U203	MMBD352L-ROHS	DUAL SCHOTTKY DIODE	3-00538
U204	MMBD352L-ROHS	DUAL SCHOTTKY DIODE	3-00538
U205	MMBD352L-ROHS	DUAL SCHOTTKY DIODE	3-00538
U206	74LVC1G3157DBVR	SPDT Analog Switch	3-02015
U207	74LVC1G3157DBVR	SPDT Analog Switch	3-02015
U208	74LVC1G3157DBVR	SPDT Analog Switch	3-02015
U209	ADA4860-1YRJZ	Current FB Op-amp	3-02003
U210	ADA4860-1YRJZ	Current FB Op-amp	3-02003
U211	ADA4860-1YRJZ	Current FB Op-amp	3-02003
U212	74HCT4053PW	Triple 2:1 Analog MPX	3-01997
U213	74LVC1GX04DCKR	Crystal Driver	3-01998
U214	LP5900SD-3.3	Low noise regulator	3-01784
U215	AD9852AST	200 MSPS DDS	3-01122
U216	ADTL082ARMZ	Dual Op amp	3-02006
U217	ADF4002BRUZ	RF PLL synthesizer	3-01755
U218	TS5A623157DGS	Dual SPDT Analog switch	3-02017
U300	MCF52235CAL60	Coldfire CPU	3-01676
U301	74HCT4051PW	8:1 Analog MPX	3-01996
U302	J1011F21PNL	Connector	1-01292
U303	74HCT4051PW	8:1 Analog MPX	3-01996
U304	74HCT4051PW	8:1 Analog MPX	3-01996
U305	74LVC3G04DCTR	Triple inverter	3-01999
U306	65LVDS2DBV	LVDS Receiver	3-01770
U307	TLV2371IDBVR	Single R-R Op Amp	3-02016
U308	74LVC138APWT	1:8 Decoder	3-01779
U309	74LVC138APWT	1:8 Decoder	3-01779
U310	M25PE80-VMN6TP	8MBit serial flash	3-02313
U311	ADM3202ARUZ	RS232 Interface Driver	3-01757
U312	74LVC2G08DCT	Single 2-input AND gate	3-01656
U313	65LVDS2DBV	LVDS Receiver	3-01770
U314	74LVC1G125DBV	Single tri-state buffer	3-01886
U315	74LVC3G04DCTR	Triple inverter	3-01999
U316	TNT4882-BQ	GPIB	3-01019
U317	74HC595ADT	Shift Register/Latch	3-00672
U318	74LVC245APWR	Octal transceiver	3-01777
U319	74HC595ADT	Shift Register/Latch	3-00672
U320	LTC2620CGN	Octal 12-bit DAC	3-01185
U321	74LVC2G08DCT	Single 2-input AND gate	3-01656
U322	74HC595ADT	Shift Register/Latch	3-00672
U323	74LVC3G04DCTR	Triple inverter	3-01999

U324	DS1816R-20	3.3V Reset, Open Drain	3-02084
U400	CY62167DV30LL-5	16 Mbit SRAM	3-02007
U401	XC3S400A-4FG320	Xilinx FPGA	3-02018
U402	TE28F320J3D75A	32 Mbit Flash	3-02009
U403	74LVC1G3157DBVR	SPDT Analog Switch	3-02015
U404	74LVC1G3157DBVR	SPDT Analog Switch	3-02015
U405	74LVC1G3157DBVR	SPDT Analog Switch	3-02015
U406	74LVC1G125DBV	Single tri-state buffer	3-01886
U407	74LVC1G3157DBVR	SPDT Analog Switch	3-02015
U408	74LVC1G125DBV	Single tri-state buffer	3-01886
U500	OPA2354AIDGKR	100 MHz R-R Op Amp	3-02014
U501	TLV3501AIDBVT	Fast R-R Comparator	3-01782
U502	LTC2227CUH#TRPB	12-bit 40 MSPS ADC	3-02012
U503	74LVC1G3157DBVR	SPDT Analog Switch	3-02015
U504	AD8131ARMZ	Differential Amplifier	3-02001
U505	74AUC1G74DCUR	Single D-type flip flop	3-01774
U506	74LVC1G3157DBVR	SPDT Analog Switch	3-02015
U507	AD8130ARM	Differential Amplifier	3-02000
U508	AD8131ARMZ	Differential Amplifier	3-02001
U509	DAC5672AIPFB	Dual 14-bit DACs	3-02008
U510	AD8131ARMZ	Differential Amplifier	3-02001
U511	74AUC1G74DCUR	Single D-type flip flop	3-01774
U512	74HCT4053PW	Triple 2:1 Analog MPX	3-01997
U513	DAC5672AIPFB	Dual 14-bit DACs	3-02008
U514	TS5A623157DGS	Dual SPDT Analog switch	3-02017
U515	AD8131ARMZ	Differential Amplifier	3-02001
U516	TS5A623157DGS	Dual SPDT Analog switch	3-02017
U517	AD8131ARMZ	Differential Amplifier	3-02001
U518	74AUC1G74DCUR	Single D-type flip flop	3-01774
U519	TLV3501AIDBVT	Fast R-R Comparator	3-01782
U600	AD8130ARM	Differential Amplifier	3-02000
U601	TPS7A4901DGN	LDO Adj Regulator	3-02179
U603	AD797AR	Low distortion op amp	3-01426
U604	ADF4108BCPZ	RF PLL synthesizer	3-02004
U605	AD9910BSVZ	1 GSPS DDS	3-02002
U606	DSCO1000-12	VCXO	6-00990
U700	ADA4860-1YRJZ	Current FB Op-amp	3-02003
U701	TS5A623157DGS	Dual SPDT Analog switch	3-02017
U702	LMH6552MAX/NOPB	1 GHz Diff Amp	3-02011
U703	LM321MF/NOPB	Single Op amp	3-02010
U704	LM321MF/NOPB	Single Op amp	3-02010
U705	TS5A623157DGS	Dual SPDT Analog switch	3-02017
U706	AD8131ARMZ	Differential Amplifier	3-02001
U707	LM321MF/NOPB	Single Op amp	3-02010
U708	TS5A623157DGS	Dual SPDT Analog switch	3-02017
U709	AD8131ARMZ	Differential Amplifier	3-02001
U710	TLV2371IDBVR	Single R-R Op Amp	3-02016
U711	65LVDS1DBV	LVDS Driver	3-01769
U712	65LVDS1DBV	LVDS Driver	3-01769
U713	65LVDS1DBV	LVDS Driver	3-01769
U714	65LVDS1DBV	LVDS Driver	3-01769
U800	LM393	Dual Comparator, SO-8	3-00728
U801	LP2951CMM	ADJ Regulator	3-01415
U802	LP3878SD-ADJ	ADJ Positive Regulator	3-01764
U803	LM317D2T	Adjustable Positive Regulator	3-01473
U804	LP3878SD-ADJ	ADJ Positive Regulator	3-01764
U805	ADR443ARMZ	3V Voltage Reference	3-02005
U806	LP3878SD-ADJ	ADJ Positive Regulator	3-01764
U807	LM337D2T	Adjustable Negative Regulator	3-01481
U808	LD1086D2T33TR	REG POS LDO 3.3V	3-02086
Y100	20,000,000HZ	Crystal	6-00643
Y200	19.5541 MHZ	Crystal	6-00822
Y201	19.607843 MHZ	Crystal	6-00823
Y202	19.6617 MHZ	Crystal	6-00824
Z0	1/2" CUSTOM	Hardware	0-01259
Z1	SG385 BRACKET	Fabricated component	7-02113
Z2	SIM-PCB S/N	Label	9-01570
Z3	4-40X1/4PP	Hardware	0-00187
Z4	BUMPER	Hardware	0-00271
Z5	1.5" WIRE	Hardware	0-00772
Z6	SG385 BOT.EMI S	Fabricated component	7-02212
Z7	SHEET	Hardware	0-00140
Z8	SG385 TOP EMI S	Fabricated component	7-02211
Z300	CEM-1203(42)	Buzzer	6-00730

RF Synthesizer for SG392 and SG394 (Assembly 327)

Ref	Value	Description	SRS P/N
C100	10000P	Capacitor, 0603, X7R	5-00752
C101	4.7U - 16V X5R	Ceramic, 16V, 1206, X5R	5-00611
C102	1000P	Capacitor, 0603, NPO	5-00740
C103	.47UF 16V /0603	Ceramic, 16V, X5R	5-00659
C104	10UF / 6.3V	Ceramic, 16V, X5R	5-00657
C105	10UF / 6.3V	Ceramic, 16V, X5R	5-00657
C106	10UF / 6.3V	Ceramic, 16V, X5R	5-00657
C107	1000P	Capacitor, 0603, NPO	5-00740
C108	100000P	Capacitor, 0603, X7R	5-00764
C109	.47UF 16V /0603	Ceramic, 16V, X5R	5-00659
C110	100000P	Capacitor, 0603, X7R	5-00764
C111	100000P	Capacitor, 0603, X7R	5-00764
C112	.47UF 16V /0603	Ceramic, 16V, X5R	5-00659
C113	100000P	Capacitor, 0603, X7R	5-00764
C114	100000P	Capacitor, 0603, X7R	5-00764
C115	4.7U - 16V X5R	Ceramic, 16V, 1206, X5R	5-00611
C116	100000P	Capacitor, 0603, X7R	5-00764
C117	100P	Capacitor, 0603, NPO	5-00716
C118	100000P	Capacitor, 0603, X7R	5-00764
C119	100000P	Capacitor, 0603, X7R	5-00764
C120	470P	Capacitor, 0603, NPO	5-00732
C121	100P	Capacitor, 0603, NPO	5-00716
C122	100P	Capacitor, 0603, NPO	5-00716
C123	1000P	Capacitor, 0603, NPO	5-00740
C124	100000P	Capacitor, 0603, X7R	5-00764
C125	470P	Capacitor, 0603, NPO	5-00732
C126	15P	Capacitor, 0603, NPO	5-00696
C127	15P	Capacitor, 0603, NPO	5-00696
C128	0.1UF - PPS	Capacitor	5-00845
C129	100P	Capacitor, 0603, NPO	5-00716
C130	22P	Capacitor, 0603, NPO	5-00700
C131	100P	Capacitor, 0603, NPO	5-00716
C132	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C133	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C134	10000P	Capacitor, 0603, X7R	5-00752
C135	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C136	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C137	1000P	Capacitor, 0603, NPO	5-00740
C138	100000P	Capacitor, 0603, X7R	5-00764
C139	100000P	Capacitor, 0603, X7R	5-00764
C140	100000P	Capacitor, 0603, X7R	5-00764
C141	100000P	Capacitor, 0603, X7R	5-00764
C142	100000P	Capacitor, 0603, X7R	5-00764
C143	100000P	Capacitor, 0603, X7R	5-00764
C144	100000P	Capacitor, 0603, X7R	5-00764
C145	22P	Capacitor, 0603, NPO	5-00700
C146	100000P	Capacitor, 0603, X7R	5-00764
C147	1P	Capacitor, 0603, NPO	5-00668
C150	100P	Capacitor, 0603, NPO	5-00716
C151	100P	Capacitor, 0603, NPO	5-00716
C200	100000P	Capacitor, 0603, X7R	5-00764
C201	1000P	Capacitor, 0603, NPO	5-00740
C202	100000P	Capacitor, 0603, X7R	5-00764
C203	100P	Capacitor, 0603, NPO	5-00716
C204	100P	Capacitor, 0603, NPO	5-00716
C205	100P	Capacitor, 0603, NPO	5-00716
C206	100P	Capacitor, 0603, NPO	5-00716
C207	100P	Capacitor, 0603, NPO	5-00716
C208	1000P	Capacitor, 0603, NPO	5-00740
C209	100000P	Capacitor, 0603, X7R	5-00764
C210	100000P	Capacitor, 0603, X7R	5-00764
C211	100000P	Capacitor, 0603, X7R	5-00764
C212	100000P	Capacitor, 0603, X7R	5-00764
C213	100000P	Capacitor, 0603, X7R	5-00764
C214	1000P	Capacitor, 0603, NPO	5-00740
C215	100P	Capacitor, 0603, NPO	5-00716
C216	100P	Capacitor, 0603, NPO	5-00716
C217	100P	Capacitor, 0603, NPO	5-00716
C218	1000P	Capacitor, 0603, NPO	5-00740

C219	100P	Capacitor, 0603, NPO	5-00716
C220	1000P	Capacitor, 0603, NPO	5-00740
C221	100000P	Capacitor, 0603, X7R	5-00764
C222	100000P	Capacitor, 0603, X7R	5-00764
C223	100000P	Capacitor, 0603, X7R	5-00764
C224	10000P	Capacitor, 0603, X7R	5-00752
C225	1000P	Capacitor, 0603, NPO	5-00740
C226	10000P	Capacitor, 0603, X7R	5-00752
C227	100000P	Capacitor, 0603, X7R	5-00764
C228	100000P	Capacitor, 0603, X7R	5-00764
C229	10000P	Capacitor, 0603, X7R	5-00752
C230	10000P	Capacitor, 0603, X7R	5-00752
C231	10000P	Capacitor, 0603, X7R	5-00752
C232	100000P	Capacitor, 0603, X7R	5-00764
C233	100000P	Capacitor, 0603, X7R	5-00764
C234	100000P	Capacitor, 0603, X7R	5-00764
C235	10000P	Capacitor, 0603, X7R	5-00752
C236	10000P	Capacitor, 0603, X7R	5-00752
C237	100000P	Capacitor, 0603, X7R	5-00764
C238	100000P	Capacitor, 0603, X7R	5-00764
C239	10000P	Capacitor, 0603, X7R	5-00752
C240	10000P	Capacitor, 0603, X7R	5-00752
C241	100000P	Capacitor, 0603, X7R	5-00764
C242	10000P	Capacitor, 0603, X7R	5-00752
D100	BAV99WT1	Diode Dual Series	3-02099
D101	BAV99WT1	Diode Dual Series	3-02099
D102	BAV99WT1	Diode Dual Series	3-02099
J100	24 PIN	Connector	1-01269
J101	34 PIN	Connector	1-01272
J200	1 PIN	Connector	1-01268
J201	1 PIN RECEPT	Connector	1-01326
L100	2506031517Y0	Inductor BEAD 0603	6-00759
L101	2506031517Y0	Inductor BEAD 0603	6-00759
L102	270NH	Fixed inductor	6-00784
L103	2506031517Y0	Inductor BEAD 0603	6-00759
L104	2506031517Y0	Inductor BEAD 0603	6-00759
L105	2506031517Y0	Inductor BEAD 0603	6-00759
L106	2506031517Y0	Inductor BEAD 0603	6-00759
L107	2506031517Y0	Inductor BEAD 0603	6-00759
L109	2506031517Y0	Inductor BEAD 0603	6-00759
L110	2506031517Y0	Inductor BEAD 0603	6-00759
L200	22NH	Inductor SMD 22nH	6-00999
L201	2506031517Y0	Inductor BEAD 0603	6-00759
L202	22NH	Inductor SMD 22nH	6-00999
L203	2506031517Y0	Inductor BEAD 0603	6-00759
L204	2506031517Y0	Inductor BEAD 0603	6-00759
L205	2506031517Y0	Inductor BEAD 0603	6-00759
L206	2506031517Y0	Inductor BEAD 0603	6-00759
L207	2506031517Y0	Inductor BEAD 0603	6-00759
L208	2506031517Y0	Inductor BEAD 0603	6-00759
L209	2506031517Y0	Inductor BEAD 0603	6-00759
L210	2506031517Y0	Inductor BEAD 0603	6-00759
PC1	SG385 RF SYNTH	Fabricated component	7-02100
R100	4.02K	Resistor, 0603, Thin Film	4-02215
R101	2.32K	Resistor, 0603, Thin Film	4-02192
R102	100	Resistor, 0603, Thin Film	4-02061
R103	1.00K	Resistor, 0603, Thin Film	4-02157
R104	1.00K	Resistor, 0603, Thin Film	4-02157
R105	49.9K	Resistor, 0603, Thin Film	4-02320
R106	10.0K	Resistor, 0603, Thin Film	4-02253
R107	10.0K	Resistor, 0603, Thin Film	4-02253
R108	100	Resistor, 0603, Thin Film	4-02061
R109	10.0K	Resistor, 0603, Thin Film	4-02253
R110	1.00K	Resistor, 0603, Thin Film	4-02157
R111	1.00K	Resistor, 0603, Thin Film	4-02157
R112	499	Resistor, 0603, Thin Film	4-02128
R113	200	Resistor, 0603, Thin Film	4-02090
R114	100	Resistor, 0603, Thin Film	4-02061
R115	49.9	Resistor, 0603, Thin Film	4-02032
R116	100	Resistor, 0603, Thin Film	4-02061
R117	4.99K	Resistor, 0603, Thin Film	4-02224
R118	249	Resistor, 0603, Thin Film	4-02099
R119	1.00K	Resistor, 0603, Thin Film	4-02157
R120	1.00K	Resistor, 0603, Thin Film	4-02157
R121	1.00K	Resistor, 0603, Thin Film	4-02157
R122	1.00K	Resistor, 0603, Thin Film	4-02157
R123	499	Resistor, 0603, Thin Film	4-02128
R124	1.00K	Resistor, 0603, Thin Film	4-02157
R125	249	Resistor, 0603, Thin Film	4-02099
R126	100	Resistor, 0603, Thin Film	4-02061
R127	49.9	Resistor, 0603, Thin Film	4-02032
R128	100	Resistor, 0603, Thin Film	4-02061
R129	100	Resistor, 0603, Thin Film	4-02061
R130	604	Resistor, 0603, Thin Film	4-02136
R131	124	Resistor, 0603, Thin Film	4-02070
R132	100	Resistor, 0603, Thin Film	4-02061
R133	604	Resistor, 0603, Thin Film	4-02136
R134	590	Resistor, 0603, Thin Film	4-02135
R135	499	Resistor, 0603, Thin Film	4-02128
R136	10.0K	Resistor, 0603, Thin Film	4-02253
R137	200	Resistor, 0603, Thin Film	4-02090
R138	301	Resistor, 0603, Thin Film	4-02107
R139	200	Resistor, 0603, Thin Film	4-02090
R140	604	Resistor, 0603, Thin Film	4-02136
R141	75	Resistor, 0603, Thin Film	4-02049
R142	750	Resistor, 0603, Thin Film	4-02145
R143	750	Resistor, 0603, Thin Film	4-02145
R144	4.99K	Resistor, 0603, Thin Film	4-02224
R200	22.1	Resistor, Thin Film, MELF	4-00958
R201	49.9	Resistor, 0603, Thin Film	4-02032
R202	150	Resistor, 0603, Thin Film	4-02078
R203	150	Resistor, 0603, Thin Film	4-02078
R204	49.9	Resistor, 0603, Thin Film	4-02032
R205	10	Resistor, 0603, Thin Film	4-01965
R206	24.9	Resistor, 0603, Thin Film	4-02003
R207	24.9	Resistor, 0603, Thin Film	4-02003
R208	49.9	Resistor, 0603, Thin Film	4-02032
R209	1.00K	Resistor, 0603, Thin Film	4-02157
R210	49.9	Resistor, 0603, Thin Film	4-02032
R211	2.00K	Resistor, 0603, Thin Film	4-02186
R212	49.9	Resistor, 0603, Thin Film	4-02032
R213	150	Resistor, 0603, Thin Film	4-02078
R214	150	Resistor, 0603, Thin Film	4-02078
R215	150	Resistor, 0603, Thin Film	4-02078
R216	150	Resistor, 0603, Thin Film	4-02078
R217	49.9	Resistor, 0603, Thin Film	4-02032
R218	49.9	Resistor, 0603, Thin Film	4-02032
R219	1.00K	Resistor, 0603, Thin Film	4-02157
R220	1.00K	Resistor, 0603, Thin Film	4-02157
R221	2.00K	Resistor, 0603, Thin Film	4-02186
R222	2.00K	Resistor, 0603, Thin Film	4-02186
R223	49.9	Resistor, 0603, Thin Film	4-02032
R224	100	Resistor, 0603, Thin Film	4-02061
R225	750	Resistor, 0603, Thin Film	4-02145
R226	49.9	Resistor, 0603, Thin Film	4-02032
R227	49.9	Resistor, 0603, Thin Film	4-02032
R228	100	Resistor, 0603, Thin Film	4-02061
R229	49.9	Resistor, 0603, Thin Film	4-02032
R230	49.9	Resistor, 0603, Thin Film	4-02032
R231	100	Resistor, 0603, Thin Film	4-02061
R232	200	Resistor, 0603, Thin Film	4-02090
R233	100	Resistor, 0603, Thin Film	4-02061
R234	2.00K	Resistor, 0603, Thin Film	4-02186
R235	49.9	Resistor, 0603, Thin Film	4-02032
R236	49.9	Resistor, 0603, Thin Film	4-02032
R237	49.9	Resistor, 0603, Thin Film	4-02032
R238	100	Resistor, 0603, Thin Film	4-02061
R239	100	Resistor, 0603, Thin Film	4-02061
R240	49.9	Resistor, 0603, Thin Film	4-02032
R241	200	Resistor, 0603, Thin Film	4-02090
R242	49.9	Resistor, 0603, Thin Film	4-02032
R243	150	Resistor, 0603, Thin Film	4-02078
R244	150	Resistor, 0603, Thin Film	4-02078
R245	49.9	Resistor, 0603, Thin Film	4-02032
R246	49.9	Resistor, 0603, Thin Film	4-02032
RN100	27x4	Resistor network	4-02508
T100	TC1-1T SMT	Transformer	6-00671
U100	LP3878SD-ADJ	ADJ Positive Regulator	3-01764
U101	LP5900SD-3.3	Low noise regulator	3-01784
U102	LP3878SD-ADJ	ADJ Positive Regulator	3-01764
U103	LP5900SD-3.3	Low noise regulator	3-01784
U104	AD797AR	Low distortion op amp	3-01426
U105	DCMO190410-5	VCO 2-4 GHz	6-01002
U106	ADCLK925BCPZ	2:1 PECL Buffer	3-02026
U107	ADF4108BCPZ	RF PLL synthesizer	3-02004
U108	DG411DVZ-T	Quad SPST Analog Switch	3-02035

U109	TLV271DBVR	Single R-R Op Amp	3-02048
U110	MC7805CDTG	5V Voltage regulator	3-02041
U111	MC79M05CDTG	5V Voltage regulator	3-02042
U112	74HC595ADT	Shift Register/Latch	3-00672
U113	74HC595ADT	Shift Register/Latch	3-00672
U114	74LVC2G08DCT	Single 2-input AND gate	3-01656
U115	LM45CIM3	Centigrade Temp Sensor	3-00775
U116	74LVC2G04	Dual inverting buffer	3-01968
U117	65LVDS2DBV	LVDS Receiver	3-01770
U118	65LVDS2DBV	LVDS Receiver	3-01770
U119	AD8131ARMZ	Differential Amplifier	3-02001
U120	TLV3501AIDBVT	Fast R-R Comparator	3-01782
U200	ADCLK925BCPZ	2:1 PECL Buffer	3-02026
U201	HMC311SC70E	RF Gain Block	3-02098
U202	LFCN-3800	FILTER LP 3.8GHz	6-00996
U203	74LVC3G34DCTR	Triple non-inverting buffer	3-01852
U204	LFCN-2000	FILTER LP 2GHz	6-00995
U205	MC100EP05	2-input PECL AND gate	3-02039
U206	HMC361S8G	DC-10 GHz Divide by two	3-02033
U207	74LVC3G34DCTR	Triple non-inverting buffer	3-01852
U208	LFCN-900	FILTER LP 900MHz	6-00998
U209	MC100EP32DTR2G	PECL 4 GHz Divide by two	3-02085
U210	LFCN-400	FILTER LP 400MHz	6-00997
U211	HMC322LP4	SP8T Non-reflective MPX	3-02031
U212	MC100EP32DTR2G	PECL 4 GHz Divide by two	3-02085
U213	74HCT4053PW	Triple 2:1 Analog MPX	3-01997
U214	LFCN-180	FILTER LP 180MHz	6-00994
U215	MC100EP32DTR2G	PECL 4 GHz Divide by two	3-02085
U216	HMC322LP4	SP8T Non-reflective MPX	3-02031
U217	LFCN-80	FILTER LP 80MHz SMD	6-01010
U218	MC100EP32DTR2G	PECL 4 GHz Divide by two	3-02085
Z0	SIM-PCB S/N	Label	9-01570

RF Synthesizer for SG396 (Assembly 333)

Ref	Value	Description	SRS P/N
C100	10000P	Capacitor, 0603, X7R	5-00752
C101	4.7U - 16V X5R	Ceramic, 16V, 1206, X5R	5-00611
C102	1000P	Capacitor, 0603, NPO	5-00740
C103	.47UF 16V /0603	Ceramic, 16V, X5R	5-00659
C104	10UF / 6.3V	Ceramic, 16V, X5R	5-00657
C105	10UF / 6.3V	Ceramic, 16V, X5R	5-00657
C106	10UF / 6.3V	Ceramic, 16V, X5R	5-00657
C107	1000P	Capacitor, 0603, NPO	5-00740
C108	100000P	Capacitor, 0603, X7R	5-00764
C109	.47UF 16V /0603	Ceramic, 16V, X5R	5-00659
C110	100000P	Capacitor, 0603, X7R	5-00764
C111	100000P	Capacitor, 0603, X7R	5-00764
C112	.47UF 16V /0603	Ceramic, 16V, X5R	5-00659
C113	100000P	Capacitor, 0603, X7R	5-00764
C114	100000P	Capacitor, 0603, X7R	5-00764
C115	4.7U - 16V X5R	Ceramic, 16V, 1206, X5R	5-00611
C116	100000P	Capacitor, 0603, X7R	5-00764
C117	100P	Capacitor, 0603, NPO	5-00716
C118	100000P	Capacitor, 0603, X7R	5-00764
C119	100000P	Capacitor, 0603, X7R	5-00764
C120	330P	Capacitor, 0603, NPO	5-00728
C121	220P	Capacitor, 0603, NPO	5-00724
C122	100P	Capacitor, 0603, NPO	5-00716
C123	1000P	Capacitor, 0603, NPO	5-00740
C124	100000P	Capacitor, 0603, X7R	5-00764
C125	100P	Capacitor, 0603, NPO	5-00716
C126	15P	Capacitor, 0603, NPO	5-00696
C127	15P	Capacitor, 0603, NPO	5-00696
C128	.047U	SMD PPS Film	5-00462
C129	100P	Capacitor, 0603, NPO	5-00716
C130	22P	Capacitor, 0603, NPO	5-00700
C131	100P	Capacitor, 0603, NPO	5-00716
C132	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C133	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C134	10000P	Capacitor, 0603, X7R	5-00752
C135	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C136	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C137	1000P	Capacitor, 0603, NPO	5-00740
C138	100000P	Capacitor, 0603, X7R	5-00764
C139	100000P	Capacitor, 0603, X7R	5-00764
C140	100000P	Capacitor, 0603, X7R	5-00764
C141	100000P	Capacitor, 0603, X7R	5-00764
C142	100000P	Capacitor, 0603, X7R	5-00764
C143	100000P	Capacitor, 0603, X7R	5-00764
C144	100000P	Capacitor, 0603, X7R	5-00764
C145	22P	Capacitor, 0603, NPO	5-00700
C146	100000P	Capacitor, 0603, X7R	5-00764
C147	1P	Capacitor, 0603, NPO	5-00668
C148	10P	Capacitor, 0603, NPO	5-00692
C149	10P	Capacitor, 0603, NPO	5-00692
C150	100P	Capacitor, 0603, NPO	5-00716
C151	100P	Capacitor, 0603, NPO	5-00716
C203	100P	Capacitor, 0603, NPO	5-00716
C205	100P	Capacitor, 0603, NPO	5-00716
C206	100P	Capacitor, 0603, NPO	5-00716
C208	1000P	Capacitor, 0603, NPO	5-00740
C210	100000P	Capacitor, 0603, X7R	5-00764
C211	100000P	Capacitor, 0603, X7R	5-00764
C212	100000P	Capacitor, 0603, X7R	5-00764
C214	1000P	Capacitor, 0603, NPO	5-00740
C215	100P	Capacitor, 0603, NPO	5-00716
C216	100P	Capacitor, 0603, NPO	5-00716
C217	100P	Capacitor, 0603, NPO	5-00716
C218	1000P	Capacitor, 0603, NPO	5-00740
C219	100P	Capacitor, 0603, NPO	5-00716
C220	1000P	Capacitor, 0603, NPO	5-00740
C221	100000P	Capacitor, 0603, X7R	5-00764
C222	100000P	Capacitor, 0603, X7R	5-00764
C223	100000P	Capacitor, 0603, X7R	5-00764
C224	10000P	Capacitor, 0603, X7R	5-00752
C226	10000P	Capacitor, 0603, X7R	5-00752
C227	100000P	Capacitor, 0603, X7R	5-00764
C228	100000P	Capacitor, 0603, X7R	5-00764
C229	10000P	Capacitor, 0603, X7R	5-00752
C230	10000P	Capacitor, 0603, X7R	5-00752
C231	10000P	Capacitor, 0603, X7R	5-00752
C232	100000P	Capacitor, 0603, X7R	5-00764
C233	100000P	Capacitor, 0603, X7R	5-00764
C234	100000P	Capacitor, 0603, X7R	5-00764
C235	10000P	Capacitor, 0603, X7R	5-00752
C236	10000P	Capacitor, 0603, X7R	5-00752
C237	100000P	Capacitor, 0603, X7R	5-00764
C238	100000P	Capacitor, 0603, X7R	5-00764
C239	10000P	Capacitor, 0603, X7R	5-00752
C240	10000P	Capacitor, 0603, X7R	5-00752
C241	100000P	Capacitor, 0603, X7R	5-00764
C242	10000P	Capacitor, 0603, X7R	5-00752
C243	100P	Capacitor, 0603, NPO	5-00716
C244	100000P	Capacitor, 0603, X7R	5-00764
C245	1000P	Capacitor, 0603, NPO	5-00740
C246	1000P	Capacitor, 0603, NPO	5-00740
C247	1000P	Capacitor, 0603, NPO	5-00740
C248	1000P	Capacitor, 0603, NPO	5-00740
C249	1000P	Capacitor, 0603, NPO	5-00740
C251	100P	Capacitor, 0603, NPO	5-00716
C252	100000P	Capacitor, 0603, X7R	5-00764
C253	100000P	Capacitor, 0603, X7R	5-00764
C254	1000P	Capacitor, 0603, NPO	5-00740
C255	100000P	Capacitor, 0603, X7R	5-00764
C257	1P	Capacitor, 0603, NPO	5-00668
C259	100P	Capacitor, 0603, NPO	5-00716
C260	100P	Capacitor, 0603, NPO	5-00716
D100	BAV99WT1	Diode Dual Series	3-02099
D101	BAV99WT1	Diode Dual Series	3-02099
D102	BAV99WT1	Diode Dual Series	3-02099
J100	24 PIN	Connector	1-01269
J101	34 PIN	Connector	1-01272
J200	1 PIN	Connector	1-01268
J201	1 PIN RECEPT	Connector	1-01326
L100	2506031517Y0	Inductor BEAD 0603	6-00759
L101	2506031517Y0	Inductor BEAD 0603	6-00759
L102	270NH	Fixed inductor	6-00784

L103	2506031517Y0	Inductor BEAD 0603	6-00759
L104	2506031517Y0	Inductor BEAD 0603	6-00759
L105	2506031517Y0	Inductor BEAD 0603	6-00759
L106	2506031517Y0	Inductor BEAD 0603	6-00759
L107	2506031517Y0	Inductor BEAD 0603	6-00759
L109	2506031517Y0	Inductor BEAD 0603	6-00759
L110	2506031517Y0	Inductor BEAD 0603	6-00759
L204	2506031517Y0	Inductor BEAD 0603	6-00759
L205	2506031517Y0	Inductor BEAD 0603	6-00759
L206	2506031517Y0	Inductor BEAD 0603	6-00759
L207	2506031517Y0	Inductor BEAD 0603	6-00759
L208	2506031517Y0	Inductor BEAD 0603	6-00759
L209	2506031517Y0	Inductor BEAD 0603	6-00759
L210	2506031517Y0	Inductor BEAD 0603	6-00759
L211	2506031517Y0	Inductor BEAD 0603	6-00759
L212	10NH	Fixed inductor	6-00681
L213	3.3 nH	Fixed inductor	6-01071
M1	2-56X3/16 HEX	Hardware	0-00764
M2	2-56X3/16 HEX	Hardware	0-00764
M3	2-56X3/16 HEX	Hardware	0-00764
M4	2-56X3/16 HEX	Hardware	0-00764
M5	2-56X3/16 HEX	Hardware	0-00764
PC1	SG386 RF Synthe	Fabricated component	7-02292
Q100	MMBT3906LT1	PNP Transistor	3-00580
R100	4.02K	Resistor, 0603, Thin Film	4-02215
R101	2.32K	Resistor, 0603, Thin Film	4-02192
R102	100	Resistor, 0603, Thin Film	4-02061
R103	1.00K	Resistor, 0603, Thin Film	4-02157
R104	1.00K	Resistor, 0603, Thin Film	4-02157
R105	49.9K	Resistor, 0603, Thin Film	4-02320
R106	10.0K	Resistor, 0603, Thin Film	4-02253
R107	10.0K	Resistor, 0603, Thin Film	4-02253
R108	100	Resistor, 0603, Thin Film	4-02061
R109	10.0K	Resistor, 0603, Thin Film	4-02253
R110	1.00K	Resistor, 0603, Thin Film	4-02157
R111	1.00K	Resistor, 0603, Thin Film	4-02157
R112	499	Resistor, 0603, Thin Film	4-02128
R113	200	Resistor, 0603, Thin Film	4-02090
R114	100	Resistor, 0603, Thin Film	4-02061
R115	49.9	Resistor, 0603, Thin Film	4-02032
R116	100	Resistor, 0603, Thin Film	4-02061
R117	2.00K	Resistor, 0603, Thin Film	4-02186
R118	249	Resistor, 0603, Thin Film	4-02099
R119	2.00K	Resistor, 0603, Thin Film	4-02186
R120	1.00K	Resistor, 0603, Thin Film	4-02157
R121	1.00K	Resistor, 0603, Thin Film	4-02157
R122	1.00K	Resistor, 0603, Thin Film	4-02157
R123	1.00K	Resistor, 0603, Thin Film	4-02157
R124	1.00K	Resistor, 0603, Thin Film	4-02157
R125	499	Resistor, 0603, Thin Film	4-02128
R126	249	Resistor, 0603, Thin Film	4-02099
R127	49.9	Resistor, 0603, Thin Film	4-02032
R128	100	Resistor, 0603, Thin Film	4-02061
R129	100	Resistor, 0603, Thin Film	4-02061
R130	604	Resistor, 0603, Thin Film	4-02136
R131	124	Resistor, 0603, Thin Film	4-02070
R132	100	Resistor, 0603, Thin Film	4-02061
R133	604	Resistor, 0603, Thin Film	4-02136
R134	590	Resistor, 0603, Thin Film	4-02135
R135	499	Resistor, 0603, Thin Film	4-02128
R136	10.0K	Resistor, 0603, Thin Film	4-02253
R137	200	Resistor, 0603, Thin Film	4-02090
R138	301	Resistor, 0603, Thin Film	4-02107
R139	200	Resistor, 0603, Thin Film	4-02090
R140	604	Resistor, 0603, Thin Film	4-02136
R141	75	Resistor, 0603, Thin Film	4-02049
R142	750	Resistor, 0603, Thin Film	4-02145
R143	750	Resistor, 0603, Thin Film	4-02145
R144	4.99K	Resistor, 0603, Thin Film	4-02224
R145	68.1K	Resistor, 0603, Thin Film	4-02333
R219	1.00K	Resistor, 0603, Thin Film	4-02157
R220	1.00K	Resistor, 0603, Thin Film	4-02157
R223	49.9	Resistor, 0603, Thin Film	4-02032
R224	100	Resistor, 0603, Thin Film	4-02061
R228	100	Resistor, 0603, Thin Film	4-02061
R229	49.9	Resistor, 0603, Thin Film	4-02032
R230	49.9	Resistor, 0603, Thin Film	4-02032
R231	100	Resistor, 0603, Thin Film	4-02061
R232	200	Resistor, 0603, Thin Film	4-02090
R233	100	Resistor, 0603, Thin Film	4-02061
R234	2.00K	Resistor, 0603, Thin Film	4-02186
R235	49.9	Resistor, 0603, Thin Film	4-02032
R236	49.9	Resistor, 0603, Thin Film	4-02032
R237	49.9	Resistor, 0603, Thin Film	4-02032
R238	100	Resistor, 0603, Thin Film	4-02061
R239	100	Resistor, 0603, Thin Film	4-02061
R240	49.9	Resistor, 0603, Thin Film	4-02032
R241	200	Resistor, 0603, Thin Film	4-02090
R242	49.9	Resistor, 0603, Thin Film	4-02032
R243	150	Resistor, 0603, Thin Film	4-02078
R244	150	Resistor, 0603, Thin Film	4-02078
R245	49.9	Resistor, 0603, Thin Film	4-02032
R246	49.9	Resistor, 0603, Thin Film	4-02032
R250	24.9	Resistor, 0603, Thin Film	4-02003
R251	24.9	Resistor, 0603, Thin Film	4-02003
R252	49.9	Resistor, 0603, Thin Film	4-02032
R253	49.9	Resistor, 0603, Thin Film	4-02032
R254	49.9	Resistor, 0603, Thin Film	4-02032
R255	24.9	Resistor, 0603, Thin Film	4-02003
R256	24.9	Resistor, 0603, Thin Film	4-02003
R257	24.9	Resistor, 0603, Thin Film	4-02003
R258	1.00K	Resistor, 0603, Thin Film	4-02157
R259	1.00K	Resistor, 0603, Thin Film	4-02157
R260	249	Resistor, 0603, Thin Film	4-02099
R261	10	Resistor, 0603, Thin Film	4-01965
R262	17.8	Resistor, 0603, Thin Film	4-01989
R263	301	Resistor, 0603, Thin Film	4-02107
R264	301	Resistor, 0603, Thin Film	4-02107
RN100	27x4	Resistor network	4-02508
RN200	8x50	Resistor network	4-02513
RN201	8x50	Resistor network	4-02513
RN202	8x50	Resistor network	4-02513
T100	TC1-1T SMT	Transformer	6-00671
U100	LP3878SD-ADJ	ADJ Positive Regulator	3-01764
U101	LP5900SD-3.3	Low noise regulator	3-01784
U102	LP3878SD-ADJ	ADJ Positive Regulator	3-01764
U103	LP5900SD-3.3	Low noise regulator	3-01784
U104	AD797AR	Low distortion op amp	3-01426
U105	DCYS300600-5	Voltage Controlled Crystal Oscillator	6-01018
U107	ADF4108BCPZ	RF PLL synthesizer	3-02004
U108	DG411DVZ-T	Quad SPST Analog Switch	3-02035
U109	TLV271DBVR	Single R-R Op Amp	3-02048
U110	MC7805CDTG	5V Voltage regulator	3-02041
U111	MC79M05CDTG	5V Voltage regulator	3-02042
U112	74HC595ADT	Shift Register/Latch	3-00672
U113	74HC595ADT	Shift Register/Latch	3-00672
U114	74LVC2G08DCT	Single 2-input AND gate	3-01656
U115	LM45CIM3	Centigrade Temp Sensor	3-00775
U116	74LVC2G04	Dual inverting buffer	3-01968
U117	65LVDS2DBV	LVDS Receiver	3-01770
U118	65LVDS2DBV	LVDS Receiver	3-01770
U119	AD8131ARMZ	Differential Amplifier	3-02001
U120	TLV3501AIDBVT	Fast R-R Comparator	3-01782
U121	ADCLK944BCPZ	Quad PECL Fanout	3-02182
U201	SKY65013-92LF	RF Gain Block	3-02043
U202	LFCN-6000	FILTER LP 6GHz	6-01026
U203	74LVC3G34DCTR	Triple non-inverting buffer	3-01852
U204	LFCN-2850	RF LOW PASS FILTER	6-01050
U206	HMC361S8G	DC-10 GHz Divide by two	3-02033
U207	74LVC3G34DCTR	Triple non-inverting buffer	3-01852
U208	LFCN-1400	RF LOW PASS FILTER	6-01049
U209	MC100EP32DTR2G	PECL 4 GHz Divide by two	3-02085
U210	LFCN-630	RF LOW PASS FILTER	6-01048
U211	HMC322LP4	SP8T Non-reflective MPX	3-02031
U212	MC100EP32DTR2G	PECL 4 GHz Divide by two	3-02085
U213	74HCT4053PW	Triple 2:1 Analog MPX	3-01997
U214	LFCN-320	RF LOW PASS FILTER	6-01047
U215	MC100EP32DTR2G	PECL 4 GHz Divide by two	3-02085
U216	HMC322LP4	SP8T Non-reflective MPX	3-02031
U217	LFCN-120	RF LOW PASS FILTER	6-01046
U218	MC100EP32DTR2G	PECL 4 GHz Divide by two	3-02085
U219	74LVC3G34DCTR	Triple non-inverting buffer	3-01852
U221	SKY65013-92LF	RF Gain Block	3-02043
U222	ADCLK925BCPZ	2:1 PECL Buffer	3-02026
Z0	SIM-PCB S/N	Label	9-01570

RF Output for SG392 and SG394. (Assembly 328)

Ref	Value	Description	SRS P/N
C100	100000P	Capacitor, 0603, X7R	5-00764
C101	100000P	Capacitor, 0603, X7R	5-00764
C102	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C103	4.7U - 16V X5R	Ceramic, 16V, 1206, X5R	5-00611
C104	4.7U - 16V X5R	Ceramic, 16V, 1206, X5R	5-00611
C105	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C106	100000P	Capacitor, 0603, X7R	5-00764
C107	100000P	Capacitor, 0603, X7R	5-00764
C108	100000P	Capacitor, 0603, X7R	5-00764
C109	10P	Capacitor, 0603, NPO	5-00692
C110	33P	Capacitor, 0603, NPO	5-00704
C111	100P	Capacitor, 0603, NPO	5-00716
C112	100P	Capacitor, 0603, NPO	5-00716
C113	10000P	SM0603, COG	5-00869
C114	10000P	SM0603, COG	5-00869
C115	100000P	Capacitor, 0603, X7R	5-00764
C116	2200P	Capacitor, 0603, X7R	5-00744
C117	100000P	Capacitor, 0603, X7R	5-00764
C118	10000P	SM0603, COG	5-00869
C119	10000P	SM0603, COG	5-00869
C120	2200P	Capacitor, 0603, X7R	5-00744
C121	1000P	Capacitor, 0603, NPO	5-00740
C122	1000P	Capacitor, 0603, NPO	5-00740
C123	100000P	Capacitor, 0603, X7R	5-00764
C124	1000P	Capacitor, 0603, NPO	5-00740
C125	100000P	Capacitor, 0603, X7R	5-00764
C126	100000P	Capacitor, 0603, X7R	5-00764
C127	100000P	Capacitor, 0603, X7R	5-00764
C128	10000P	SM0603, COG	5-00869
C129	100000P	Capacitor, 0603, X7R	5-00764
C130	100000P	Capacitor, 0603, X7R	5-00764
C131	100000P	Capacitor, 0603, X7R	5-00764
C132	100000P	Capacitor, 0603, X7R	5-00764
C133	100000P	Capacitor, 0603, X7R	5-00764
C200	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C201	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C202	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C203	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C204	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C205	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C206	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C207	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C208	100000P	Capacitor, 0603, X7R	5-00764
C209	100000P	Capacitor, 0603, X7R	5-00764
C210	100000P	Capacitor, 0603, X7R	5-00764
C211	100000P	Capacitor, 0603, X7R	5-00764
C212	10000P	SM0603, COG	5-00869
C213	10000P	SM0603, COG	5-00869
C214	10000P	SM0603, COG	5-00869
C215	10000P	SM0603, COG	5-00869
C216	10000P	SM0603, COG	5-00869
C217	100P	Capacitor, 0603, NPO	5-00716
C218	100P	Capacitor, 0603, NPO	5-00716
C220	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C224	390P	Capacitor, 0603, NPO	5-00730
C225	390P	Capacitor, 0603, NPO	5-00730
C226	390P	Capacitor, 0603, NPO	5-00730
C227	390P	Capacitor, 0603, NPO	5-00730
C228	1000P	Capacitor, 0603, NPO	5-00740
C229	1000P	Capacitor, 0603, NPO	5-00740
C300	100000P	Capacitor, 0603, X7R	5-00764
C301	100000P	Capacitor, 0603, X7R	5-00764
C302	100000P	Capacitor, 0603, X7R	5-00764
C303	100000P	Capacitor, 0603, X7R	5-00764
C304	100000P	Capacitor, 0603, X7R	5-00764
C305	33P	Capacitor, 0603, NPO	5-00704
C306	33P	Capacitor, 0603, NPO	5-00704
C307	100000P	Capacitor, 0603, X7R	5-00764
C308	100000P	Capacitor, 0603, X7R	5-00764
C309	100000P	Capacitor, 0603, X7R	5-00764
C310	100P	Capacitor, 0603, NPO	5-00716
C311	1000P	Capacitor, 0603, NPO	5-00740
C312	100000P	Capacitor, 0603, X7R	5-00764
C313	33P	Capacitor, 0603, NPO	5-00704
C314	33P	Capacitor, 0603, NPO	5-00704
CN100	4X0.1uF	cap net 4 x 0.1uf	5-00842
CN200	4X0.1uF	cap net 4 x 0.1uf	5-00842
CN201	4X0.1uF	cap net 4 x 0.1uf	5-00842
CN202	4X0.1uF	cap net 4 x 0.1uf	5-00842
CN203	4X0.1uF	cap net 4 x 0.1uf	5-00842
CN204	4-100PF	cap net 4 x 100pf	5-00843
CN205	4-100PF	cap net 4 x 100pf	5-00843
CN206	4-100PF	cap net 4 x 100pf	5-00843
CN207	4-100PF	cap net 4 x 100pf	5-00843
D100	BAV99WT1	Diode Dual Series	3-02099
D200	BAV99WT1	Diode Dual Series	3-02099
D201	BAV99WT1	Diode Dual Series	3-02099
D202	BAV99WT1	Diode Dual Series	3-02099
D203	BAV99WT1	Diode Dual Series	3-02099
D204	FLZ5V6B	DIODE ZENER 5.6V	3-02080
J100	1 PIN	Connector	1-01267
J101	24 PIN	Connector	1-01270
L100	2506031517Y0	Inductor BEAD 0603	6-00759
L101	2506031517Y0	Inductor BEAD 0603	6-00759
L102	33UH - SMT	Inductor, 1210, Ferrite	6-00654
L103	.47UH - SMT	Inductor, 1210, Iron	6-00650
L104	82nH	INDUCTOR 82NH	6-01009
L105	2506031517Y0	Inductor BEAD 0603	6-00759
L106	1.8uH	Fixed inductor	6-01004
L107	2506031517Y0	Inductor BEAD 0603	6-00759
L108	2506031517Y0	Inductor BEAD 0603	6-00759
L109	2506031517Y0	Inductor BEAD 0603	6-00759
L110	2506031517Y0	Inductor BEAD 0603	6-00759
L200	22NH	Inductor SMD 22nH	6-00999
L201	2506031517Y0	Inductor BEAD 0603	6-00759
L202	22NH	Inductor SMD 22nH	6-00999
L203	2506031517Y0	Inductor BEAD 0603	6-00759
L204	22NH	Inductor SMD 22nH	6-00999
L205	2506031517Y0	Inductor BEAD 0603	6-00759
L206	22NH	Inductor SMD 22nH	6-00999
L207	2506031517Y0	Inductor BEAD 0603	6-00759
L208	33UH - SMT	Inductor, 1210, Ferrite	6-00654
L209	33UH - SMT	Inductor, 1210, Ferrite	6-00654
L210	.47UH - SMT	Inductor, 1210, Iron	6-00650
L211	.47UH - SMT	Inductor, 1210, Iron	6-00650
L212	82nH	INDUCTOR 82NH	6-01009
L213	82nH	INDUCTOR 82NH	6-01009
L300	2506031517Y0	Inductor BEAD 0603	6-00759
L301	2506031517Y0	Inductor BEAD 0603	6-00759
L302	2506031517Y0	Inductor BEAD 0603	6-00759
L303	150NH	Fixed inductor	6-00989
L304	2506031517Y0	Inductor BEAD 0603	6-00759
L305	150NH	Fixed inductor	6-00989
PC1	SG385 RF OUTPUT	Fabricated component	7-02101
R100	1.00K	Resistor, 0603, Thin Film	4-02157
R102	100	Resistor, 0603, Thin Film	4-02061
R103	100	Resistor, 0603, Thin Film	4-02061
R104	649K	Resistor, 0603, Thin Film	4-02427
R105	49.9	Resistor, 0603, Thin Film	4-02032
R106	49.9	Resistor, 0603, Thin Film	4-02032
R107	499	Resistor, 0603, Thin Film	4-02128
R108	100	Resistor, 0603, Thin Film	4-02061
R109	100	Resistor, 0603, Thin Film	4-02061
R110	100	Resistor, 0603, Thin Film	4-02061
R111	100	Resistor, 0603, Thin Film	4-02061
R112	100	Resistor, 0603, Thin Film	4-02061
R113	100	Resistor, 0603, Thin Film	4-02061
R114	100	Resistor, 0603, Thin Film	4-02061
R115	100	Resistor, 0603, Thin Film	4-02061
R116	49.9	Resistor, 0603, Thin Film	4-02032
R117	499	Resistor, 0603, Thin Film	4-02128
R118	499	Resistor, 0603, Thin Film	4-02128
R119	499	Resistor, 0603, Thin Film	4-02128
R120	1.00K	Resistor, 0603, Thin Film	4-02157
R121	499	Resistor, 0603, Thin Film	4-02128
R122	1.00K	Resistor, 0603, Thin Film	4-02157
R124	499	Resistor, 0603, Thin Film	4-02128

R125	20.0K	Resistor, 0603, Thin Film	4-02282
R126	10.0K	Resistor, 0603, Thin Film	4-02253
R127	17.8	Resistor, 0603, Thin Film	4-01989
R128	301	Resistor, 0603, Thin Film	4-02107
R129	301	Resistor, 0603, Thin Film	4-02107
R130	499	Resistor, 0603, Thin Film	4-02128
R131	499	Resistor, 0603, Thin Film	4-02128
R132	49.9	Resistor, 0603, Thin Film	4-02032
R133	49.9	Resistor, 0603, Thin Film	4-02032
R134	4.02K	Resistor, 0603, Thin Film	4-02215
R135	4.02K	Resistor, 0603, Thin Film	4-02215
R136	4.02K	Resistor, 0603, Thin Film	4-02215
R137	4.02K	Resistor, 0603, Thin Film	4-02215
R138	49.9	Resistor, 0603, Thin Film	4-02032
R139	49.9	Resistor, 0603, Thin Film	4-02032
R140	100	Resistor, 0603, Thin Film	4-02061
R141	49.9	Resistor, 0603, Thin Film	4-02032
R142	49.9	Resistor, 0603, Thin Film	4-02032
R143	24.9	Resistor, 0603, Thin Film	4-02003
R144	2.00K	Resistor, 0603, Thin Film	4-02186
R145	4.02K	Resistor, 0603, Thin Film	4-02215
R146	1.00K	Resistor, 0603, Thin Film	4-02157
R147	10.0K	Resistor, 0603, Thin Film	4-02253
R148	100	Resistor, 0603, Thin Film	4-02061
R149	100K	Resistor, 0603, Thin Film	4-02349
R150	100K	Resistor, 0603, Thin Film	4-02349
R151	100	Resistor, 0603, Thin Film	4-02061
R200	49.9	Resistor, 0603, Thin Film	4-02032
R201	49.9	Resistor, 0603, Thin Film	4-02032
R202	24.9	Resistor, 0603, Thin Film	4-02003
R203	24.9	Resistor, 0603, Thin Film	4-02003
R204	499	Resistor, 0603, Thin Film	4-02128
R205	499	Resistor, 0603, Thin Film	4-02128
R206	499	Resistor, 0603, Thin Film	4-02128
R207	499	Resistor, 0603, Thin Film	4-02128
R208	499	Resistor, 0603, Thin Film	4-02128
R209	499	Resistor, 0603, Thin Film	4-02128
R210	20.0K	Resistor, 0603, Thin Film	4-02282
R211	20.0K	Resistor, 0603, Thin Film	4-02282
R212	10.0K	Resistor, 0603, Thin Film	4-02253
R213	20.0K	Resistor, 0603, Thin Film	4-02282
R214	4.99K	Resistor, 0603, Thin Film	4-02224
R215	4.99K	Resistor, 0603, Thin Film	4-02224
R216	1.50K	Resistor, 0603, Thin Film	4-02174
R217	499	Resistor, 0603, Thin Film	4-02128
R218	499	Resistor, 0603, Thin Film	4-02128
R224	2.00K	Resistor, 0603, Thin Film	4-02186
R225	2.00K	Resistor, 0603, Thin Film	4-02186
R300	604	Resistor, 0603, Thin Film	4-02136
R301	49.9	Resistor, 0603, Thin Film	4-02032
R302	768	Resistor, 0603, Thin Film	4-02146
R303	301	Resistor, 0603, Thin Film	4-02107
R304	499	Resistor, 0603, Thin Film	4-02128
R305	49.9 / 1W	Surface mount, Power	4-02510
R306	53.6	Resistor, 0603, Thin Film	4-02035
R307	24.9	Resistor, 0603, Thin Film	4-02003
R308	604	Resistor, 0603, Thin Film	4-02136
R309	49.9	Resistor, 0603, Thin Film	4-02032
R310	49.9	Resistor, 0603, Thin Film	4-02032
R311	100	Resistor, 0603, Thin Film	4-02061
R312	10.0K	Resistor, 0603, Thin Film	4-02253
R313	10.0K	Resistor, 0603, Thin Film	4-02253
R314	2.00K	Resistor, 0603, Thin Film	4-02186
R315	301	Resistor, 0603, Thin Film	4-02107
R316	1.00K	Resistor, 0603, Thin Film	4-02157
R317	10.0K	Resistor, 0603, Thin Film	4-02253
R318	10.0K	Resistor, 0603, Thin Film	4-02253
R319	10.0K	Resistor, 0603, Thin Film	4-02253
R320	1.00K	Resistor, 0603, Thin Film	4-02157
R321	100K	Resistor, 0603, Thin Film	4-02349
R322	100K	Resistor, 0603, Thin Film	4-02349
R323	750	Resistor, 0603, Thin Film	4-02145
R324	100	Resistor, 0603, Thin Film	4-02061
R325	100	Resistor, 0603, Thin Film	4-02061
RN100	742C083151J	Resistor array, 4x150	4-02454
RN200	742C083151J	Resistor array, 4x150	4-02454
RN201	742C083151J	Resistor array, 4x150	4-02454
RN202	742C083151J	Resistor array, 4x150	4-02454
U100	74HCT4053PW	Triple 2:1 Analog MPX	3-01997
U101	74HCT4053PW	Triple 2:1 Analog MPX	3-01997
U102	LT3080	LDO POS Adj regulator	3-02036
U103	HMC270MS8GE	SPDT Non-reflect Switch	3-02030
U104	HMC270MS8GE	SPDT Non-reflect Switch	3-02030
U105	HMC270MS8GE	SPDT Non-reflect Switch	3-02030
U106	HMC270MS8GE	SPDT Non-reflect Switch	3-02030
U107	HMC624LP4	RF Atten dig 31.5dB	3-02082
U109	SKY65014-92LF	RF Gain Block	3-02044
U110	ADL5375-05ACPZ	I-Q RF Modulator	3-02028
U111	HMC346MS8G	VC RF atten	3-02032
U112	HMC346MS8G	VC RF atten	3-02032
U113	TLV2372IDGK	Dual RRIO CMOS Op-Amp	3-01434
U114	AD8130ARM	Differential Amplifier	3-02000
U115	74HC595ADT	Shift Register/Latch	3-00672
U116	74LVC1G125DBV	Single tri-state buffer	3-01886
U117	TLV2372IDGK	Dual RRIO CMOS Op-Amp	3-01434
U200	LT2630CSC6-HZ8	DAC Serial 8-bit	3-02083
U201	HMC624LP4	RF Atten dig 31.5dB	3-02082
U202	HMC624LP4	RF Atten dig 31.5dB	3-02082
U203	HMC624LP4	RF Atten dig 31.5dB	3-02082
U204	HMC624LP4	RF Atten dig 31.5dB	3-02082
U205	SKY65014-92LF	RF Gain Block	3-02044
U206	SKY65017	RF Gain Block	3-02045
U300	OPA2695IDR	1 GHz CFB Op amp	3-02089
U301	TS5A623157DGS	Dual SPDT Analog switch	3-02017
U302	TS5A623157DGS	Dual SPDT Analog switch	3-02017
U303	AD8130ARM	Differential Amplifier	3-02000
U304	DAT-31	RF Step attenuator	3-02050
U305	74LVC1G3157	SPST Analog switch	3-02046
U306	TLV2371IDBVR	Single R-R Op Amp	3-02016
Z0	SIM-PCB S/N	Label	9-01570

RF Output for SG396 (Assembly 334)

Ref	Value	Description	SRS P/N
C100	100000P	Capacitor, 0603, X7R	5-00764
C101	100000P	Capacitor, 0603, X7R	5-00764
C102	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C103	4.7U - 16V X5R	Ceramic, 16V, 1206, X5R	5-00611
C104	4.7U - 16V X5R	Ceramic, 16V, 1206, X5R	5-00611
C105	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C106	100000P	Capacitor, 0603, X7R	5-00764
C107	100000P	Capacitor, 0603, X7R	5-00764
C108	100000P	Capacitor, 0603, X7R	5-00764
C109	10P	Capacitor, 0603, NPO	5-00692
C110	33P	Capacitor, 0603, NPO	5-00704
C111	100P	Capacitor, 0603, NPO	5-00716
C112	100P	Capacitor, 0603, NPO	5-00716
C113	100000P	Capacitor, 0603, X7R	5-00764
C114	10000P	SM0603, COG	5-00869
C115	100000P	Capacitor, 0603, X7R	5-00764
C116	2200P	Capacitor, 0603, X7R	5-00744
C117	100000P	Capacitor, 0603, X7R	5-00764
C118	10000P	SM0603, COG	5-00869
C119	10000P	SM0603, COG	5-00869
C120	2200P	Capacitor, 0603, X7R	5-00744
C121	1000P	Capacitor, 0603, NPO	5-00740
C122	1000P	Capacitor, 0603, NPO	5-00740
C123	100000P	Capacitor, 0603, X7R	5-00764
C124	1000P	Capacitor, 0603, NPO	5-00740
C125	100000P	Capacitor, 0603, X7R	5-00764
C126	100000P	Capacitor, 0603, X7R	5-00764
C127	100000P	Capacitor, 0603, X7R	5-00764
C128	10000P	SM0603, COG	5-00869
C129	100000P	Capacitor, 0603, X7R	5-00764
C130	100000P	Capacitor, 0603, X7R	5-00764
C131	100000P	Capacitor, 0603, X7R	5-00764
C132	100000P	Capacitor, 0603, X7R	5-00764
C133	100000P	Capacitor, 0603, X7R	5-00764

C200	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C201	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C202	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C203	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C204	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C205	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C206	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C207	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C208	100000P	Capacitor, 0603, X7R	5-00764
C209	100000P	Capacitor, 0603, X7R	5-00764
C210	100000P	Capacitor, 0603, X7R	5-00764
C211	100000P	Capacitor, 0603, X7R	5-00764
C212	10000P	SM0603, COG	5-00869
C213	10000P	SM0603, COG	5-00869
C214	10000P	SM0603, COG	5-00869
C215	10000P	SM0603, COG	5-00869
C216	10000P	SM0603, COG	5-00869
C217	100P	Capacitor, 0603, NPO	5-00716
C218	100P	Capacitor, 0603, NPO	5-00716
C220	1UF 16V /0603	Ceramic, 16V, 0603, X5R	5-00661
C224	390P	Capacitor, 0603, NPO	5-00730
C225	390P	Capacitor, 0603, NPO	5-00730
C226	390P	Capacitor, 0603, NPO	5-00730
C227	390P	Capacitor, 0603, NPO	5-00730
C228	1000P	Capacitor, 0603, NPO	5-00740
C229	1000P	Capacitor, 0603, NPO	5-00740
C250	10000P	SM0603, COG	5-00869
C251	10000P	SM0603, COG	5-00869
C252	10000P	SM0603, COG	5-00869
C253	10000P	SM0603, COG	5-00869
C254	10000P	SM0603, COG	5-00869
C255	10000P	SM0603, COG	5-00869
C300	100000P	Capacitor, 0603, X7R	5-00764
C301	100000P	Capacitor, 0603, X7R	5-00764
C302	100000P	Capacitor, 0603, X7R	5-00764
C303	100000P	Capacitor, 0603, X7R	5-00764
C304	100000P	Capacitor, 0603, X7R	5-00764
C305	33P	Capacitor, 0603, NPO	5-00704
C306	33P	Capacitor, 0603, NPO	5-00704
C307	100000P	Capacitor, 0603, X7R	5-00764
C308	100000P	Capacitor, 0603, X7R	5-00764
C309	100000P	Capacitor, 0603, X7R	5-00764
C310	100P	Capacitor, 0603, NPO	5-00716
C311	1000P	Capacitor, 0603, NPO	5-00740
C312	100000P	Capacitor, 0603, X7R	5-00764
C313	33P	Capacitor, 0603, NPO	5-00704
C314	33P	Capacitor, 0603, NPO	5-00704
CN100	4X0.1uF	cap net 4 x 0.1uf	5-00842
CN200	4X0.1uF	cap net 4 x 0.1uf	5-00842
CN201	4X0.1uF	cap net 4 x 0.1uf	5-00842
CN202	4X0.1uF	cap net 4 x 0.1uf	5-00842
CN203	4X0.1uF	cap net 4 x 0.1uf	5-00842
CN204	4-100PF	cap net 4 x 100pf	5-00843
CN205	4-100PF	cap net 4 x 100pf	5-00843
CN206	4-100PF	cap net 4 x 100pf	5-00843
CN207	4-100PF	cap net 4 x 100pf	5-00843
D100	BAV99WT1	Diode Dual Series	3-02099
D200	BAV99WT1	Diode Dual Series	3-02099
D201	BAV99WT1	Diode Dual Series	3-02099
D202	BAV99WT1	Diode Dual Series	3-02099
D203	BAV99WT1	Diode Dual Series	3-02099
D204	FLZ5V6B	DIODE ZENER 5.6V	3-02080
J100	1 PIN	Connector	1-01267
J101	24 PIN	Connector	1-01270
J200	172117	Connector	1-01265
J300	73100-0195	Panel Mount BNC	1-01158
L100	2506031517Y0	Inductor BEAD 0603	6-00759
L101	2506031517Y0	Inductor BEAD 0603	6-00759
L102	33UH - SMT	Inductor, 1210, Ferrite	6-00654
L103	.47UH - SMT	Inductor, 1210, Iron	6-00650
L104	82nH	INDUCTOR 82NH	6-01009
L105	2506031517Y0	Inductor BEAD 0603	6-00759
L106	1.8uH	Fixed inductor	6-01004
L107	2506031517Y0	Inductor BEAD 0603	6-00759
L108	2506031517Y0	Inductor BEAD 0603	6-00759
L109	2506031517Y0	Inductor BEAD 0603	6-00759
L110	2506031517Y0	Inductor BEAD 0603	6-00759
L200	22NH	Inductor SMD 22nH	6-00999

L201	2506031517Y0	Inductor BEAD 0603	6-00759
L202	22NH	Inductor SMD 22nH	6-00999
L203	2506031517Y0	Inductor BEAD 0603	6-00759
L204	22NH	Inductor SMD 22nH	6-00999
L205	2506031517Y0	Inductor BEAD 0603	6-00759
L206	22NH	Inductor SMD 22nH	6-00999
L207	2506031517Y0	Inductor BEAD 0603	6-00759
L209	33UH - SMT	Inductor, 1210, Ferrite	6-00654
L211	.47UH - SMT	Inductor, 1210, Iron	6-00650
L213	82nH	INDUCTOR 82NH	6-01009
L250	33UH - SMT	Inductor, 1210, Ferrite	6-00654
L251	33UH - SMT	Inductor, 1210, Ferrite	6-00654
L300	2506031517Y0	Inductor BEAD 0603	6-00759
L301	2506031517Y0	Inductor BEAD 0603	6-00759
L302	2506031517Y0	Inductor BEAD 0603	6-00759
L303	150NH	Fixed inductor	6-00989
L304	2506031517Y0	Inductor BEAD 0603	6-00759
L305	150NH	Fixed inductor	6-00989
M100	2-56X3/16 HEX	Hardware	0-00764
M101	2-56X3/16 HEX	Hardware	0-00764
M102	2-56X3/16 HEX	Hardware	0-00764
M103	2-56X3/16 HEX	Hardware	0-00764
M200	2-56X3/16 HEX	Hardware	0-00764
M201	2-56X3/16 HEX	Hardware	0-00764
M202	2-56X3/16 HEX	Hardware	0-00764
M203	2-56X3/16 HEX	Hardware	0-00764
M204	2-56X3/16 HEX	Hardware	0-00764
M205	2-56X3/16 HEX	Hardware	0-00764
M206	2-56X3/16 HEX	Hardware	0-00764
M207	2-56X3/16 HEX	Hardware	0-00764
M208	2-56X3/16 HEX	Hardware	0-00764
M209	2-56X3/16 HEX	Hardware	0-00764
PC1	SG386 RF AMPL	Fabricated component	7-02293
R100	1.00K	Resistor, 0603, Thin Film	4-02157
R102	100	Resistor, 0603, Thin Film	4-02061
R103	100	Resistor, 0603, Thin Film	4-02061
R104	649K	Resistor, 0603, Thin Film	4-02427
R105	49.9	Resistor, 0603, Thin Film	4-02032
R106	49.9	Resistor, 0603, Thin Film	4-02032
R107	499	Resistor, 0603, Thin Film	4-02128
R108	100	Resistor, 0603, Thin Film	4-02061
R109	100	Resistor, 0603, Thin Film	4-02061
R110	100	Resistor, 0603, Thin Film	4-02061
R111	100	Resistor, 0603, Thin Film	4-02061
R112	100	Resistor, 0603, Thin Film	4-02061
R113	100	Resistor, 0603, Thin Film	4-02061
R114	100	Resistor, 0603, Thin Film	4-02061
R115	100	Resistor, 0603, Thin Film	4-02061
R116	49.9	Resistor, 0603, Thin Film	4-02032
R117	499	Resistor, 0603, Thin Film	4-02128
R118	499	Resistor, 0603, Thin Film	4-02128
R119	499	Resistor, 0603, Thin Film	4-02128
R120	1.00K	Resistor, 0603, Thin Film	4-02157
R121	499	Resistor, 0603, Thin Film	4-02128
R122	1.00K	Resistor, 0603, Thin Film	4-02157
R124	499	Resistor, 0603, Thin Film	4-02128
R125	20.0K	Resistor, 0603, Thin Film	4-02282
R126	10.0K	Resistor, 0603, Thin Film	4-02253
R127	17.8	Resistor, 0603, Thin Film	4-01989
R128	301	Resistor, 0603, Thin Film	4-02107
R129	301	Resistor, 0603, Thin Film	4-02107
R130	499	Resistor, 0603, Thin Film	4-02128
R131	499	Resistor, 0603, Thin Film	4-02128
R132	49.9	Resistor, 0603, Thin Film	4-02032
R133	49.9	Resistor, 0603, Thin Film	4-02032
R134	4.02K	Resistor, 0603, Thin Film	4-02215
R135	4.02K	Resistor, 0603, Thin Film	4-02215
R136	4.02K	Resistor, 0603, Thin Film	4-02215
R137	4.02K	Resistor, 0603, Thin Film	4-02215
R138	49.9	Resistor, 0603, Thin Film	4-02032
R139	49.9	Resistor, 0603, Thin Film	4-02032
R140	100	Resistor, 0603, Thin Film	4-02061
R141	49.9	Resistor, 0603, Thin Film	4-02032
R142	49.9	Resistor, 0603, Thin Film	4-02032
R143	24.9	Resistor, 0603, Thin Film	4-02003
R144	2.00K	Resistor, 0603, Thin Film	4-02186
R145	4.02K	Resistor, 0603, Thin Film	4-02215
R146	1.00K	Resistor, 0603, Thin Film	4-02157

R147	10.0K	Resistor, 0603, Thin Film	4-02253
R148	100	Resistor, 0603, Thin Film	4-02061
R149	100K	Resistor, 0603, Thin Film	4-02349
R150	100K	Resistor, 0603, Thin Film	4-02349
R151	100	Resistor, 0603, Thin Film	4-02061
R202	24.9	Resistor, 0603, Thin Film	4-02003
R203	24.9	Resistor, 0603, Thin Film	4-02003
R205	499	Resistor, 0603, Thin Film	4-02128
R207	499	Resistor, 0603, Thin Film	4-02128
R209	499	Resistor, 0603, Thin Film	4-02128
R210	20.0K	Resistor, 0603, Thin Film	4-02282
R211	20.0K	Resistor, 0603, Thin Film	4-02282
R213	20.0K	Resistor, 0603, Thin Film	4-02282
R214	4.99K	Resistor, 0603, Thin Film	4-02224
R215	4.99K	Resistor, 0603, Thin Film	4-02224
R216	1.50K	Resistor, 0603, Thin Film	4-02174
R217	499	Resistor, 0603, Thin Film	4-02128
R218	499	Resistor, 0603, Thin Film	4-02128
R224	2.00K	Resistor, 0603, Thin Film	4-02186
R225	2.00K	Resistor, 0603, Thin Film	4-02186
R250	12.4	Resistor, 0603, Thin Film	4-01974
R251	12.4	Resistor, 0603, Thin Film	4-01974
R252	12.4	Resistor, 0603, Thin Film	4-01974
R253	12.4	Resistor, 0603, Thin Film	4-01974
R254	20.0K	Resistor, 0603, Thin Film	4-02282
R255	20.0K	Resistor, 0603, Thin Film	4-02282
R300	604	Resistor, 0603, Thin Film	4-02136
R301	49.9	Resistor, 0603, Thin Film	4-02032
R302	768	Resistor, 0603, Thin Film	4-02146
R303	301	Resistor, 0603, Thin Film	4-02107
R304	499	Resistor, 0603, Thin Film	4-02128
R305	49.9 / 1W	Surface mount, Power	4-02510
R306	53.6	Resistor, 0603, Thin Film	4-02035
R307	24.9	Resistor, 0603, Thin Film	4-02003
R308	604	Resistor, 0603, Thin Film	4-02136
R309	49.9	Resistor, 0603, Thin Film	4-02032
R310	49.9	Resistor, 0603, Thin Film	4-02032
R311	100	Resistor, 0603, Thin Film	4-02061
R312	10.0K	Resistor, 0603, Thin Film	4-02253
R313	10.0K	Resistor, 0603, Thin Film	4-02253
R314	2.00K	Resistor, 0603, Thin Film	4-02186
R315	301	Resistor, 0603, Thin Film	4-02107
R316	1.00K	Resistor, 0603, Thin Film	4-02157
R317	10.0K	Resistor, 0603, Thin Film	4-02253
R318	10.0K	Resistor, 0603, Thin Film	4-02253
R319	10.0K	Resistor, 0603, Thin Film	4-02253
R320	1.00K	Resistor, 0603, Thin Film	4-02157
R321	100K	Resistor, 0603, Thin Film	4-02349
R322	100K	Resistor, 0603, Thin Film	4-02349
R323	750	Resistor, 0603, Thin Film	4-02145
R324	100	Resistor, 0603, Thin Film	4-02061
R325	100	Resistor, 0603, Thin Film	4-02061
RN100	742C083151J	Resistor array, 4x150	4-02454
RN200	742C083151J	Resistor array, 4x150	4-02454
RN201	742C083151J	Resistor array, 4x150	4-02454
RN202	742C083151J	Resistor array, 4x150	4-02454
U100	74HCT4053PW	Triple 2:1 Analog MPX	3-01997
U101	74HCT4053PW	Triple 2:1 Analog MPX	3-01997
U102	LT3080	LDO POS Adj regulator	3-02036
U103	HMC270MS8GE	SPDT Non-reflect Switch	3-02030
U104	HMC270MS8GE	SPDT Non-reflect Switch	3-02030
U105	HMC270MS8GE	SPDT Non-reflect Switch	3-02030
U106	HMC270MS8GE	SPDT Non-reflect Switch	3-02030
U107	HMC624LP4	RF Atten dig 31.5dB	3-02082
U109	SKY65014-92LF	RF Gain Block	3-02044
U110	ADL5375-05ACPZ	I-Q RF Modulator	3-02028
U111	HMC346MS8G	VC RF atten	3-02032
U112	HMC346MS8G	VC RF atten	3-02032
U113	TLV2372IDGK	Dual RRIO CMOS Op-Amp	3-01434
U114	AD8130ARM	Differential Amplifier	3-02000
U115	74HC595ADT	Shift Register/Latch	3-00672
U116	74LVC1G125DBV	Single tri-state buffer	3-01886
U117	TLV2372IDGK	Dual RRIO CMOS Op-Amp	3-01434
U200	LT2630CSC6-HZ8	DAC Serial 8-bit	3-02083
U201	HMC624LP4	RF Atten dig 31.5dB	3-02082
U202	HMC624LP4	RF Atten dig 31.5dB	3-02082
U203	HMC624LP4	RF Atten dig 31.5dB	3-02082
U204	HMC624LP4	RF Atten dig 31.5dB	3-02082
U250	SKY65014-92LF	RF Gain Block	3-02044
U251	SKY65014-92LF	RF Gain Block	3-02044
U252	HMC788LP2E	RF Gain Block	3-02168
U300	OPA2695IDR	1 GHz CFB Op amp	3-02089
U301	TS5A623157DGS	Dual SPDT Analog switch	3-02017
U302	TS5A623157DGS	Dual SPDT Analog switch	3-02017
U303	AD8130ARM	Differential Amplifier	3-02000
U304	DAT-31	RF Step attenuator	3-02050
U305	74LVC1G3157	SPST Analog switch	3-02046
U306	TLV2371IDBVR	Single R-R Op Amp	3-02016
Z0	SIM-PCB S/N	Label	9-01570

Motherboard to RF Block Jumper PCB (Assembly 329)

Ref	Value	Description	SRS P/N
C1	2.2P	Capacitor, 0603, NPO	5-00675
C2	2.2P	Capacitor, 0603, NPO	5-00675
C3	2.2P	Capacitor, 0603, NPO	5-00675
C4	2.2P	Capacitor, 0603, NPO	5-00675
C5	2.2P	Capacitor, 0603, NPO	5-00675
C6	2.2P	Capacitor, 0603, NPO	5-00675
C7	2.2P	Capacitor, 0603, NPO	5-00675
C8	2.2P	Capacitor, 0603, NPO	5-00675
C9	2.2P	Capacitor, 0603, NPO	5-00675
C10	2.2P	Capacitor, 0603, NPO	5-00675
C11	2.2P	Capacitor, 0603, NPO	5-00675
C12	2.2P	Capacitor, 0603, NPO	5-00675
C13	2.2P	Capacitor, 0603, NPO	5-00675
C14	2.2P	Capacitor, 0603, NPO	5-00675
C15	2.2P	Capacitor, 0603, NPO	5-00675
C16	2.2P	Capacitor, 0603, NPO	5-00675
C17	2.2P	Capacitor, 0603, NPO	5-00675
C18	2.2P	Capacitor, 0603, NPO	5-00675
C19	2.2P	Capacitor, 0603, NPO	5-00675
C20	2.2P	Capacitor, 0603, NPO	5-00675
C21	2.2P	Capacitor, 0603, NPO	5-00675
C22	2.2P	Capacitor, 0603, NPO	5-00675
C23	2.2P	Capacitor, 0603, NPO	5-00675
C24	2.2P	Capacitor, 0603, NPO	5-00675
C25	2.2P	Capacitor, 0603, NPO	5-00675
C26	2.2P	Capacitor, 0603, NPO	5-00675
C27	2.2P	Capacitor, 0603, NPO	5-00675
C28	2.2P	Capacitor, 0603, NPO	5-00675
C29	2.2P	Capacitor, 0603, NPO	5-00675
C30	2.2P	Capacitor, 0603, NPO	5-00675
C31	2.2P	Capacitor, 0603, NPO	5-00675
C32	2.2P	Capacitor, 0603, NPO	5-00675
C33	2.2P	Capacitor, 0603, NPO	5-00675
C34	2.2P	Capacitor, 0603, NPO	5-00675
C35	2.2P	Capacitor, 0603, NPO	5-00675
C36	2.2P	Capacitor, 0603, NPO	5-00675
C37	2.2P	Capacitor, 0603, NPO	5-00675
C38	2.2P	Capacitor, 0603, NPO	5-00675
C39	2.2P	Capacitor, 0603, NPO	5-00675
C40	2.2P	Capacitor, 0603, NPO	5-00675
C41	2.2P	Capacitor, 0603, NPO	5-00675
C42	2.2P	Capacitor, 0603, NPO	5-00675
C43	2.2P	Capacitor, 0603, NPO	5-00675
C44	2.2P	Capacitor, 0603, NPO	5-00675
C45	2.2P	Capacitor, 0603, NPO	5-00675
C46	2.2P	Capacitor, 0603, NPO	5-00675
C47	2.2P	Capacitor, 0603, NPO	5-00675
C48	2.2P	Capacitor, 0603, NPO	5-00675
C49	2.2P	Capacitor, 0603, NPO	5-00675
C50	2.2P	Capacitor, 0603, NPO	5-00675
C51	2.2P	Capacitor, 0603, NPO	5-00675
C52	2.2P	Capacitor, 0603, NPO	5-00675
C53	10000P	Capacitor, 0603, X7R	5-00752
C54	10000P	Capacitor, 0603, X7R	5-00752
C55	10000P	Capacitor, 0603, X7R	5-00752

C56	10000P	Capacitor, 0603, X7R	5-00752
C57	10000P	Capacitor, 0603, X7R	5-00752
C58	10000P	Capacitor, 0603, X7R	5-00752
C59	10000P	Capacitor, 0603, X7R	5-00752
C60	10000P	Capacitor, 0603, X7R	5-00752
J1	34 PIN	Connector	1-01275
J2	34 PIN	Connector	1-01275
L1	Choke, Common M	Common Mode Choke	6-01019
L2	Choke, Common M	Common Mode Choke	6-01019
L3	Choke, Common M	Common Mode Choke	6-01019
L4	Choke, Common M	Common Mode Choke	6-01019
L5	2506031517Y0	Inductor BEAD 0603	6-00759
L6	Choke, Common M	Common Mode Choke	6-01019
L7	Choke, Common M	Common Mode Choke	6-01019
L8	Choke, Common M	Common Mode Choke	6-01019
L9	2506031517Y0	Inductor BEAD 0603	6-00759
L10	2506031517Y0	Inductor BEAD 0603	6-00759
L11	2506031517Y0	Inductor BEAD 0603	6-00759
L12	2506031517Y0	Inductor BEAD 0603	6-00759
L13	2506031517Y0	Inductor BEAD 0603	6-00759
PCB1	SG385 MB TO RF	Fabricated component	7-02104
R1	100	Resistor, 0603, Thick Film	4-01845
R2	100	Resistor, 0603, Thick Film	4-01845
R3	100	Resistor, 0603, Thick Film	4-01845
R4	100	Resistor, 0603, Thick Film	4-01845
R5	100	Resistor, 0603, Thick Film	4-01845
R6	100	Resistor, 0603, Thick Film	4-01845
R7	100	Resistor, 0603, Thick Film	4-01845
R8	100	Resistor, 0603, Thick Film	4-01845
R9	100	Resistor, 0603, Thick Film	4-01845
R10	100	Resistor, 0603, Thick Film	4-01845
R11	100	Resistor, 0603, Thick Film	4-01845
Z0	SIM-PCB S/N	Label	9-01570

Rear Panel I/Q BNCs (Assembly 335)

Ref	Value	Description	SRS P/N
C1	100000P	Capacitor, 0603, X7R	5-00764
C2	100000P	Capacitor, 0603, X7R	5-00764
C3	100000P	Capacitor, 0603, X7R	5-00764
C4	100000P	Capacitor, 0603, X7R	5-00764
C5	100000P	Capacitor, 0603, X7R	5-00764
C6	100000P	Capacitor, 0603, X7R	5-00764
C7	100000P	Capacitor, 0603, X7R	5-00764
C8	100000P	Capacitor, 0603, X7R	5-00764
C9	100000P	Capacitor, 0603, X7R	5-00764
C10	100000P	Capacitor, 0603, X7R	5-00764
C11	100000P	Capacitor, 0603, X7R	5-00764
C12	100000P	Capacitor, 0603, X7R	5-00764
C13	100000P	Capacitor, 0603, X7R	5-00764
J1	73100-0195	Panel Mount BNC	1-01158
J2	73100-0195	Panel Mount BNC	1-01158
J3	73100-0195	Panel Mount BNC	1-01158
J4	15 PIN	Connector	1-01264
J5	73100-0195	Panel Mount BNC	1-01158
L1	2506031517Y0	Inductor BEAD 0603	6-00759
L2	2506031517Y0	Inductor BEAD 0603	6-00759
L3	2506031517Y0	Inductor BEAD 0603	6-00759
L4	2506031517Y0	Inductor BEAD 0603	6-00759
L5	2506031517Y0	Inductor BEAD 0603	6-00759
L6	2506031517Y0	Inductor BEAD 0603	6-00759
L7	2506031517Y0	Inductor BEAD 0603	6-00759
L8	2506031517Y0	Inductor BEAD 0603	6-00759
L9	2506031517Y0	Inductor BEAD 0603	6-00759
L10	2506031517Y0	Inductor BEAD 0603	6-00759
L11	2506031517Y0	Inductor BEAD 0603	6-00759
L12	2506031517Y0	Inductor BEAD 0603	6-00759
PCB1	SG385 OPT.3	Fabricated component	7-02103
R1	49.9	Resistor, 0603, Thin Film	4-02032
R2	2.00K	Resistor, 0603, Thin Film	4-02186
R3	2.00K	Resistor, 0603, Thin Film	4-02186
R4	2.00K	Resistor, 0603, Thin Film	4-02186
R5	2.00K	Resistor, 0603, Thin Film	4-02186
R6	49.9	Resistor, 0603, Thin Film	4-02032
R7	49.9	Resistor, 0603, Thin Film	4-02032
R8	1.37K	Resistor, 0603, Thin Film	4-02170
R9	1.00K	Resistor, 0603, Thin Film	4-02157
R10	1.15K	Resistor, 0603, Thin Film	4-02163
R11	2.00K	Resistor, 0603, Thin Film	4-02186
R12	2.00K	Resistor, 0603, Thin Film	4-02186
R13	1.15K	Resistor, 0603, Thin Film	4-02163
R14	10.0K	Resistor, 0603, Thin Film	4-02253
R15	49.9	Resistor, 0603, Thin Film	4-02032
R16	49.9	Resistor, 0603, Thin Film	4-02032
R17	52.3	Resistor, Thin Film, MELF	4-00994
R18	24.9	Resistor, 0603, Thin Film	4-02003
R19	49.9	Resistor, 0603, Thin Film	4-02032
R20	1.15K	Resistor, 0603, Thin Film	4-02163
R21	49.9	Resistor, 0603, Thin Film	4-02032
R22	49.9	Resistor, 0603, Thin Film	4-02032
R23	1.37K	Resistor, 0603, Thin Film	4-02170
R24	1.00K	Resistor, 0603, Thin Film	4-02157
R25	2.00K	Resistor, 0603, Thin Film	4-02186
R26	2.00K	Resistor, 0603, Thin Film	4-02186
R27	2.00K	Resistor, 0603, Thin Film	4-02186
R28	2.00K	Resistor, 0603, Thin Film	4-02186
R29	1.15K	Resistor, 0603, Thin Film	4-02163
R30	2.00K	Resistor, 0603, Thin Film	4-02186
R31	2.00K	Resistor, 0603, Thin Film	4-02186
R32	1.15K	Resistor, 0603, Thin Film	4-02163
R33	10.0K	Resistor, 0603, Thin Film	4-02253
R34	49.9	Resistor, 0603, Thin Film	4-02032
R35	49.9	Resistor, 0603, Thin Film	4-02032
R36	52.3	Resistor, Thin Film, MELF	4-00994
R37	24.9	Resistor, 0603, Thin Film	4-02003
R38	1.15K	Resistor, 0603, Thin Film	4-02163
R39	21.5K	Resistor, 0603, Thin Film	4-02285
R40	21.5K	Resistor, 0603, Thin Film	4-02285
R41	21.5K	Resistor, 0603, Thin Film	4-02285
R42	21.5K	Resistor, 0603, Thin Film	4-02285
U1	AD8130ARM	Differential Amplifier	3-02000
U2	TLV3502AIDR	R-R Comparator	3-02019
U3	74LVC32AD	Quad 2-Input OR gate	3-01087
U4	AD8131AR	Diff Amp	3-01129
U5	AD8130ARM	Differential Amplifier	3-02000
U6	65LVDS1DBV	LVDS Driver	3-01769
U7	TLV3502AIDR	R-R Comparator	3-02019
U8	AD8131AR	Diff Amp	3-01129
Z0	4-40X3/16PP	Hardware	0-00241
Z1	SIM-PCB S/N	Label	9-01570
Z2	1/2" CUSTOM	Hardware	0-01259
Z3	SG385 BRACKET	Fabricated component	7-02112

Rear Panel Sync Board (Assembly 346)

Ref	Value	Description	SRS P/N
C1	100000P	Capacitor, 0603, X7R	5-00764
C2	100000P	Capacitor, 0603, X7R	5-00764
C3	100000P	Capacitor, 0603, X7R	5-00764
C4	100000P	Capacitor, 0603, X7R	5-00764
C5	100000P	Capacitor, 0603, X7R	5-00764
C6	100000P	Capacitor, 0603, X7R	5-00764
C7	100000P	Capacitor, 0603, X7R	5-00764
C8	100000P	Capacitor, 0603, X7R	5-00764
C9	100000P	Capacitor, 0603, X7R	5-00764
C10	100000P	Capacitor, 0603, X7R	5-00764
C11	100000P	Capacitor, 0603, X7R	5-00764
C12	100000P	Capacitor, 0603, X7R	5-00764
C13	100000P	Capacitor, 0603, X7R	5-00764
C14	100000P	Capacitor, 0603, X7R	5-00764

J1	15 PIN	Connector	1-01264
J2	43860-0001	Connector	1-01380
J3	73100-0195	Panel Mount BNC	1-01158
J4	73100-0195	Panel Mount BNC	1-01158
J5	73100-0195	Panel Mount BNC	1-01158
J6	73100-0195	Panel Mount BNC	1-01158
L1	2506031517Y0	Inductor BEAD 0603	6-00759
L3	2506031517Y0	Inductor BEAD 0603	6-00759
L4	2506031517Y0	Inductor BEAD 0603	6-00759
L5	2506031517Y0	Inductor BEAD 0603	6-00759
L6	2506031517Y0	Inductor BEAD 0603	6-00759
PC1	SG390 PCB R.P.	Fabricated component	7-02406
R1	100	Resistor, 0603, Thin Film	4-02061
R2	4.7	Resistor, Thick Film, Chip	4-01423
R3	45.3	Resistor, 0603, Thin Film	4-02028
R4	100	Resistor, 0603, Thin Film	4-02061
R5	4.7	Resistor, Thick Film, Chip	4-01423
R6	100	Resistor, 0603, Thin Film	4-02061
R7	45.3	Resistor, 0603, Thin Film	4-02028
R8	4.7	Resistor, Thick Film, Chip	4-01423
R9	100	Resistor, 0603, Thin Film	4-02061
R10	45.3	Resistor, 0603, Thin Film	4-02028
R11	4.7	Resistor, Thick Film, Chip	4-01423
R12	100	Resistor, 0603, Thin Film	4-02061
R13	45.3	Resistor, 0603, Thin Film	4-02028
U1	74LVC1G157GW	Single 2-input MPX	3-01766
U2	74HCT595PW	Shift Register/Latch	3-02169
U3	74LVC1G125DBV	Single tri-state buffer	3-01886
U4	TLV3501AIDBVT	Fast R-R Comparator	3-01782
U5	74LVC1G157GW	Single 2-input MPX	3-01766
U6	SN74LVC1G08DBVR	Single AND Gate	3-01203
U7	74LVC3G34DCTR	Triple non-inverting buffer	3-01852
U8	65LVDS2DBV	LVDS Receiver	3-01770
U9	65LVDS2DBV	LVDS Receiver	3-01770
U10	74LVC2G74DCTR	Single D-type flip flop	3-01867
U11	74LVC3G34DCTR	Triple non-inverting buffer	3-01852
U12	65LVDS2DBV	LVDS Receiver	3-01770
U13	74LVC2G74DCTR	Single D-type flip flop	3-01867
U14	74LVC3G34DCTR	Triple non-inverting buffer	3-01852
U15	65LVDS2DBV	LVDS Receiver	3-01770
U16	74LVC2G74DCTR	Single D-type flip flop	3-01867
U17	74LVC3G34DCTR	Triple non-inverting buffer	3-01852
Z0	SIM-PCB S/N	Label	9-01570
Z1	1/2" CUSTOM	Hardware	0-01259
Z2	SG385 BRACKET	Fabricated component	7-02112

Power Supply (Assemblies 337 & 338)

Ref	Value	Description	SRS P/N
C1	820UF	Electrolytic, 50V, T/H	5-00844
C2	10U/T35	SMD TANTALUM, D-Case	5-00319
C3	330U HIGH RIPPL	Electrolytic, High Ripple	5-00516
C4	10U/T35	SMD TANTALUM, D-Case	5-00319
C5	1000P	Capacitor, Ceramic, 1kV	5-00143
C6	10U/T35	SMD TANTALUM, D-Case	5-00319
C7	330U HIGH RIPPL	Electrolytic, High Ripple	5-00516
C8	10U/T35	SMD TANTALUM, D-Case	5-00319
C9	1000P	Capacitor, Ceramic, 1kV	5-00143
C10	.1U	Capacitor, 1206, X7R	5-00299
C11	330U HIGH RIPPL	Electrolytic, High Ripple	5-00516
C12	10U/T35	SMD TANTALUM, D-Case	5-00319
C13	1000P	Capacitor, Ceramic, 1kV	5-00143
C14	.1U	Capacitor, 1206, X7R	5-00299
C15	330U HIGH RIPPL	Electrolytic, High Ripple	5-00516
C16	10U/T35	SMD TANTALUM, D-Case	5-00319
C17	.001U	SMD PPS Film	5-00442
C18	820UF	Electrolytic, 50V, T/H	5-00844
C19	1000P	Capacitor, Ceramic, 1kV	5-00143
C20	.01U	Capacitor, 1206, X7R	5-00298
C21	330U HIGH RIPPL	Electrolytic, High Ripple	5-00516
C22	10U/T35	SMD TANTALUM, D-Case	5-00319
C23	1000P	Capacitor, Ceramic, 1kV	5-00143
D1	RED	LED, T1 Package	3-00011
D2	ES2D	Diode, SMB, Fast	3-02090
D3	MBRS230LT3G	Diode, Schottky	3-02091
D4	ES2D	Diode, SMB, Fast	3-02090
D5	ES2D	Diode, SMB, Fast	3-02090
D6	MBRS230LT3G	Diode, Schottky	3-02091
D7	ES2D	Diode, SMB, Fast	3-02090
D8	ES2D	Diode, SMB, Fast	3-02090
D9	MBRS230LT3G	Diode, Schottky	3-02091
D10	ES2D	Diode, SMB, Fast	3-02090
D11	ES2D	Diode, SMB, Fast	3-02090
D12	MBRS230LT3G	Diode, Schottky	3-02091
D13	ES2D	Diode, SMB, Fast	3-02090
D14	ES2D	Diode, SMB, Fast	3-02090
D15	MBRS230LT3G	Diode, Schottky	3-02091
D16	ES2D	Diode, SMB, Fast	3-02090
J1	4 PIN, WHITE	Connector	1-00260
J2	HEADER10	Connector	1-00554
J3	2 PIN, WHITE	Connector	1-00473
L1	10 UH / SMT	INDUCTOR 10U 2.5A	6-01016
L2	10 UH / SMT	INDUCTOR 10U 2.5A	6-01016
L3	10 UH / SMT	INDUCTOR 10U 2.5A	6-01016
L4	10 UH / SMT	INDUCTOR 10U 2.5A	6-01016
L5	10 UH / SMT	INDUCTOR 10U 2.5A	6-01016
L6	10 UH / SMT	INDUCTOR 10U 2.5A	6-01016
L7	10 UH / SMT	INDUCTOR 10U 2.5A	6-01016
PCB1	SG385 P/S PCB	Fabricated component	7-02205
Q1	PZT3904	NPN Transistor	3-01664
Q2	IRF530/IRF532	N Channel MOSFET	3-00283
Q3	IRF530/IRF532	N Channel MOSFET	3-00283
R1	7.50K	Resistor, Thin Film, MELF	4-01201
R2	121	Resistor, Thin Film, MELF	4-01029
R3	100K	Resistor, Thin Film, MELF	4-01309
R4	2.00K	Resistor, Thin Film, MELF	4-01146
R5	1.33K	Resistor, Thin Film, MELF	4-01129
R6	49.9	Resistor, Thin Film, MELF	4-00992
R7	1.00K	Resistor, Thin Film, MELF	4-01117
R8	49.9	Resistor, Thin Film, MELF	4-00992
R9	7.50K	Resistor, Thin Film, MELF	4-01201
R10	49.9	Resistor, Thin Film, MELF	4-00992
R11	0.15 OHM /2W	Shunt, 3008 Size	4-02530
RN1	100Kx4D 5%	Resistor network	4-01704
RN2	100Kx4D 5%	Resistor network	4-01704
T1	DG645/SG385	Transformer	6-00765
U1	LM358	Dual op amp	3-00773
U2	LM45CIM3	Centigrade Temp Sensor	3-00775
U3	LM1085IT-ADJ/NO	POS ADJ voltage regulator	3-02111
U4	LM2990T-15	LDO Negative regulator	3-01787
U5	UA78L12ACPK	REG LIN POS 12V	3-02092
U6	LM1085IT-5.0/NO	Positive +5V Regulator	3-02112
U7	3525A	IC Switcher	3-00919
U8	LM2990T-5	LDO Negative regulator	3-01789
U9	LM1085IT-3.3/NO	Positive +3.3V Regulator	3-02093
Z0	5 PIN, 18AWG/OR	Connector	1-00033
Z1	1-32, #4 SHOULD	Hardware	0-00231
Z2	TO-220	Hardware	0-00243
Z3	4-40X5/16"PF	Hardware	0-00589
Z4	10-32 KEP	Hardware	0-00160
Z5	4-40X3/8PF	Hardware	0-00208
Z6	SG385 SPACER BL	Fabricated component	7-02207
Z7	AFM03	Silicone Fan Mount	0-01335
Z8	KDE1205PHV2	Fan	0-01181
Z9	3" BLACK	Wire	0-01191
Z10	3" RED	Wire	0-01192
Z11	10" WHITE	Wire	0-01231
Z12	10" BLACK	Wire	0-01238
Z13	4-40 KEP	Hardware	0-00043
Z14	6-32X1/4PP	Hardware	0-00222
Z15	13 PIN, ORANGE	Connector	1-00601
Z16	4"GREEN W/YELL	Wire	0-01014
Z17	2-520184-2	Hardware	0-00634
Z18	2 PIN, 24AWG/WH	Connector	1-00472
Z19	6-32X1/2RP	Hardware	0-00167
Z20	4-40X1/4PP	Hardware	0-00187
Z21	10-32X1/2"PP	Hardware	0-00493
Z22	4 PIN, 18AWG/OR	Connector	1-00259
Z23	SG385 INSULATOR	Fabricated component	7-02200

Z24	36154	Hardware	0-00084
Z25	SG385 P/S COVER	Fabricated component	7-02199
Z26	FN9222R-3-06	Power Entry Hardware	0-01333
Z27	SG385 P/S ENCLO	Fabricated component	7-02198
Z28	120W - 24V	OEM Power supply, +24V	6-01017
Z29	SILICONE TUBING	Hardware	0-01345

OCXO Timebase (Assembly 605)

Ref	Value	Description	SRS P/N
J1	SSW-107-01-S-S	Connector	1-01078
J3	09-52-3101	Connector	1-01058
PC1	CG635 TIMEBASE	Fabricated component	7-01586
R1	3.01K	Resistor, Metal Film	4-00176
R2	2.00K	Resistor, Metal Film	4-00158
R3	3.01K	Resistor, Metal Film	4-00176
R4	12.1K	Resistor, Metal Film	4-00148
U1	LM358	Dual OpAmp	3-00508
Z0	26-48-1101	Connector	1-01057
Z1	4-40X1/4PP	Hardware	0-00187
Z2	8-32X1/4PF	Hardware	0-00416
Z3	CG635, OPT	Fabricated component	7-01614
Z4	3403	Hardware	0-01090
Z5	6-32 KEP	Hardware	0-00048
Z6	SC10-24V - CG	Oscillator	6-00079

Option 4: Rubidium Timebase (Assembly 607)

Ref	Value	Description	SRS P/N
C1	.1U	Capacitor, Ceramic, 50V, Z5U	5-00023
J2	10 PIN STRAIGHT	Connector	1-00342
J2A	COAX CONTACT	Connector	1-00343
J3	09-52-3101	Connector	1-01058
PC1	CG635 TIMEBASE	Fabricated component	7-01586
R1	3.01K	Resistor, Metal Film	4-00176
R2	2.00K	Resistor, Metal Film	4-00158
R3	3.01K	Resistor, Metal Film	4-00176
R4	12.1K	Resistor, Metal Film	4-00148
U1	LM358	Dual OpAmp	3-00508
U2	74HC04	Hex Inverter	3-00155
U3	78L05	+5V, Low Power Regulator	3-00116
Z0	4-40 KEP	Hardware	0-00043
Z1	4-40X1/4PP	Hardware	0-00187
Z2	8-32X1/4PF	Hardware	0-00416
Z3	4-40X1/4 M/F	Hardware	0-00781
Z4	26-48-1101	Connector	1-01057
Z5	SRS RB OSC.	Oscillator	6-00159
Z6	CG635, OPT	Fabricated component	7-01614

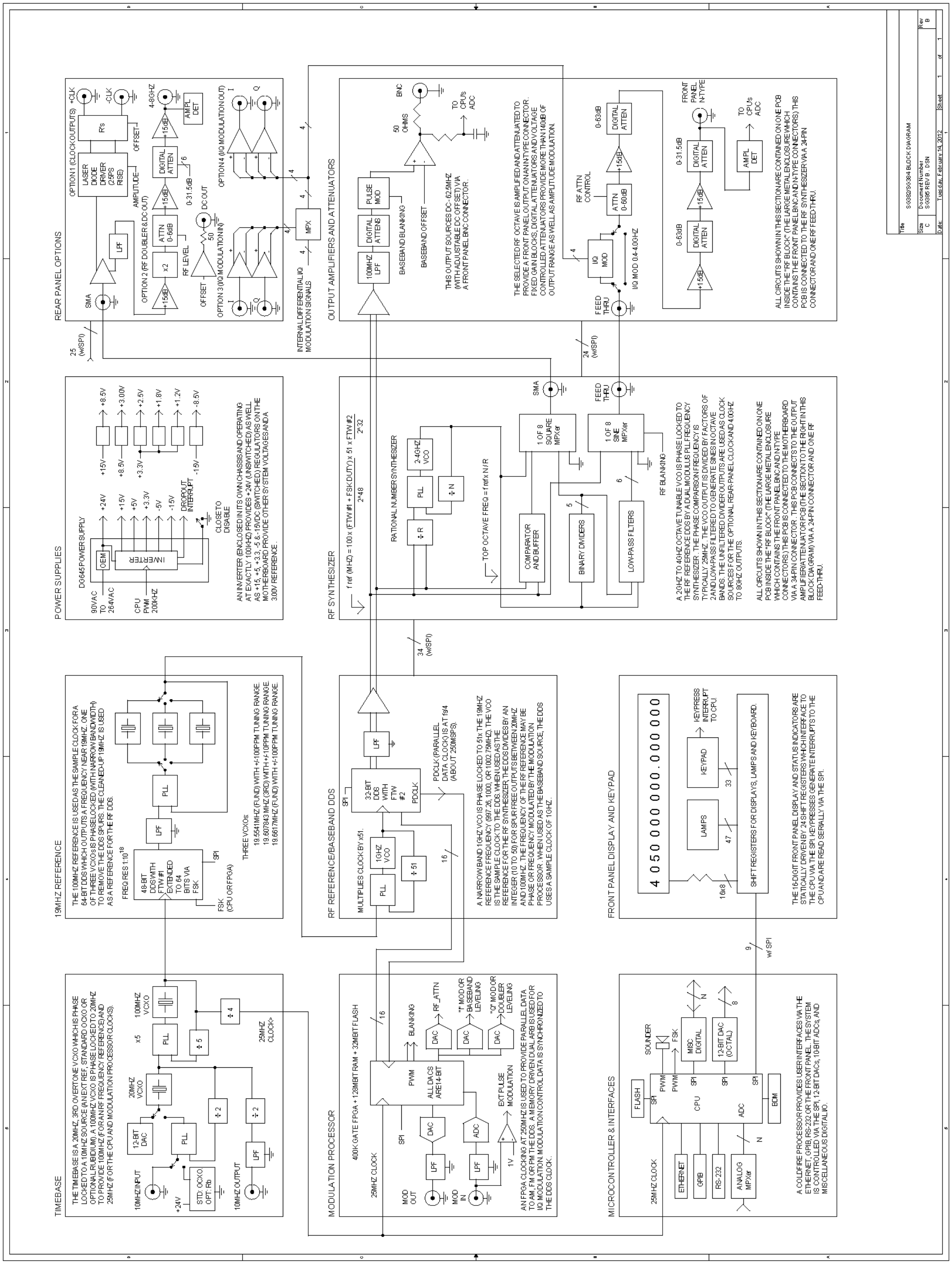
Main Chassis Kit (Assembly 347)

Ref	Value	Description	SRS P/N
J1	25 PIN	Connector	1-01277
J2	15 PIN	Connector	1-01276
J3	15 PIN	Connector	1-01276
Z0	141-14SM+	Connector	1-01335
Z1	FOOT PLUG	Hardware	0-01352
Z2	4-40 x 1/8 UNDE	Hardware	0-01334
Z3	SG385 LEXAN	Fabricated component	7-02171
Z4	SG385 EMI SHIEL	Fabricated component	7-02169
Z5	132360	Connector	1-01334
Z6	9-PIN	Connector	1-01309
Z7	SG385 CRYSTAL S	Fabricated component	7-02197
Z8	SG385 BAR RF BL	Fabricated component	7-02170
Z9	10-32 x 3/8"	Hardware	0-01331
Z10	SG, OPT.COVR	Fabricated component	7-02134
Z11	4-40X3/16PP	Hardware	0-00241
Z12	10-32X3/8TRUSSP	Hardware	0-00248
Z13	4-40X1/4PP	Hardware	0-00187
Z14	F0104	Hardware	0-00189
Z15	RIGHT FOOT	Hardware	0-00179
Z16	LEFT FOOT	Hardware	0-00180
Z17	6-32X1/2FP BLK	Hardware	0-00492
Z18	554043-1	Hardware	0-00500
Z19	4-40X3/8PF UNDR	Hardware	0-00835
Z20	6-32X1/4 BLACK	Hardware	0-01212
Z21	SG385 MB TO RP	Fabricated component	7-02105
Z22	SG385 S/N LABEL	Label	9-01641
Z23	6-32X3/8PP	Hardware	0-00185
Z24	4-40X3/16 M/F	Hardware	0-00079
Z25	4-40X1/4PF	Hardware	0-00150
Z26	DG535-36	Fabricated component	7-00122
Z27	8-32X1/4PF	Hardware	0-00242
Z28	6-32X7/16 PP	Hardware	0-00315
Z29	REAR FOOT	Hardware	0-00204
Z30	SG390, FRT BOOT	Fabricated component	7-02382
Z31	SG390, REAR BOOT	Fabricated component	7-02383
Z32	SG390, BOT. COVR	Fabricated component	7-02393
Z33	SG390 Top Cover	Fabricated component	7-02394
Z34	SG396, LEXAN	Fabricated component	7-02390
Z35	SG390 Keypad	Fabricated component	7-02391
Z36	1FT_ETHERNET	Connector	1-01394
Z37	SG390 Rear Pane	Fabricated component	7-02405
Z38	SG390 RP LEXAN	Fabricated component	7-02407
Z39	SG396, BEZEL	Fabricated component	7-02432
Z40	SG394 Lexan	Fabricated component	7-02443
Z41	SG392 Lexan	Fabricated component	7-02444
Z42	SG396, SPACER BZL	Fabricated component	7-02433

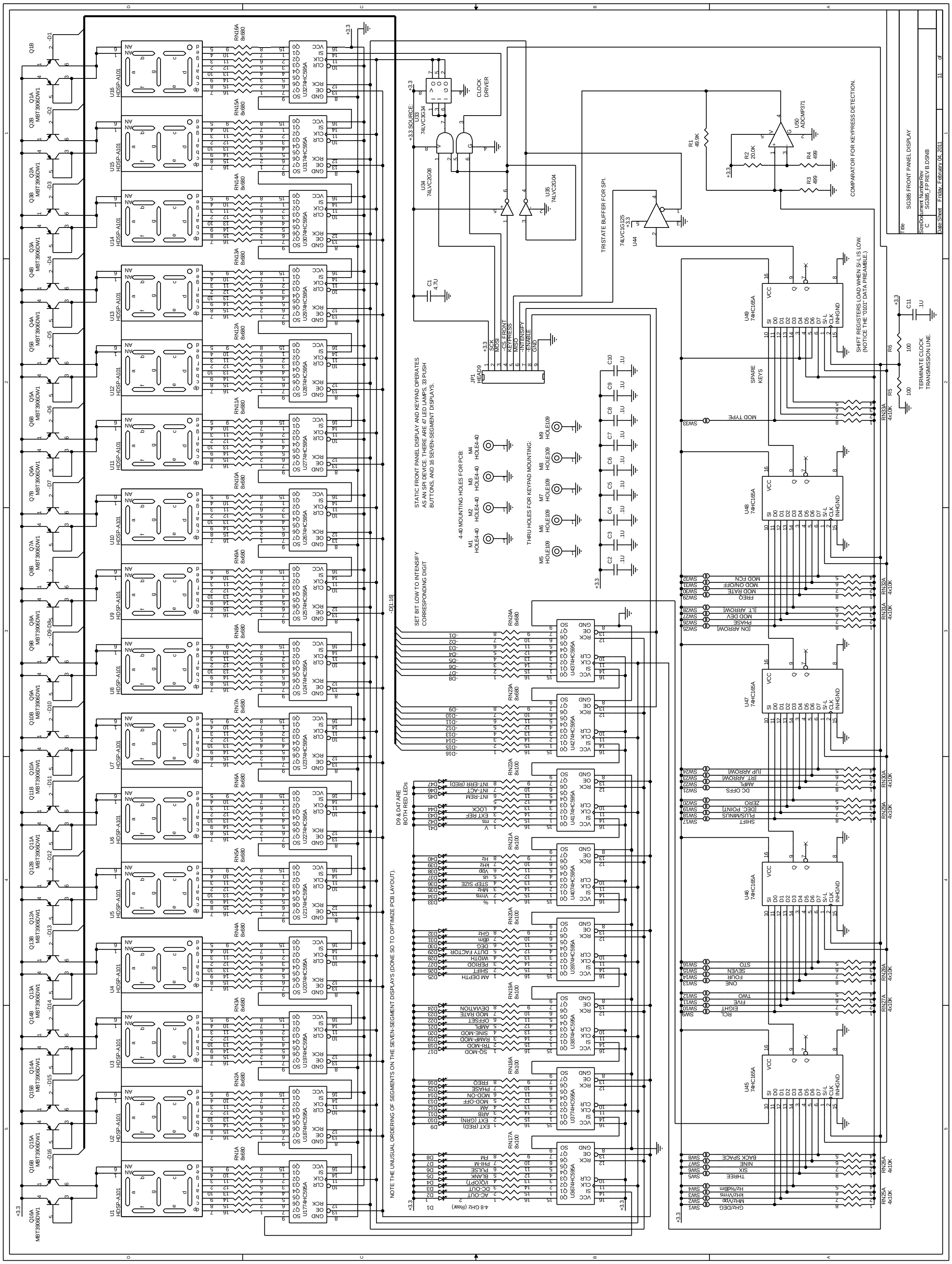
Appendix C : Schematic Diagrams

Schematic 1: Block Diagram
Schematic 2: Front Panel Display
Schematic 3: Display EMI Filter
Schematic 4: Mother Board 1, Frequency Refs
Schematic 5: Mother Board 2, 19 MHz Ref
Schematic 6: Mother Board 3, CPU
Schematic 7: Mother Board 4, Modulation Processor
Schematic 8: Mother Board 5, Modulation ADC / DACs
Schematic 9: Mother Board 6, RF Reference
Schematic 10: Mother Board 7, Interface
Schematic 11: Mother Board 8, Power Supplies
Schematic 12: Mother Board to RF Jumper
Schematic 13: SG394 Synthesizer 1, 2-4 GHz and Control
Schematic 14: SG394 Synthesizer 2, Dividers and LPF
Schematic 15: SG396 Synthesizer 1, 3-6 GHz and Control
Schematic 16: SG396 Synthesizer 2, Dividers and LPF
Schematic 17: SG394 Output 1, Attenuation & Controls
Schematic 18: SG394 Output 2, RF Stage
Schematic 19: SG394 Output 3, BNC
Schematic 20: SG396 Output 1, Attenuation & Controls
Schematic 21: SG396 Output 2, RF Stage
Schematic 22: SG396 Output 3, BNC
Schematic 23: Power Supply
Schematic 24: Rear Panel Option Jumper
Schematic 25: I/Q Modulator
Schematic 26: Symbol Clock and Event Markers
Schematic 27: Timebase Adaptor Interface

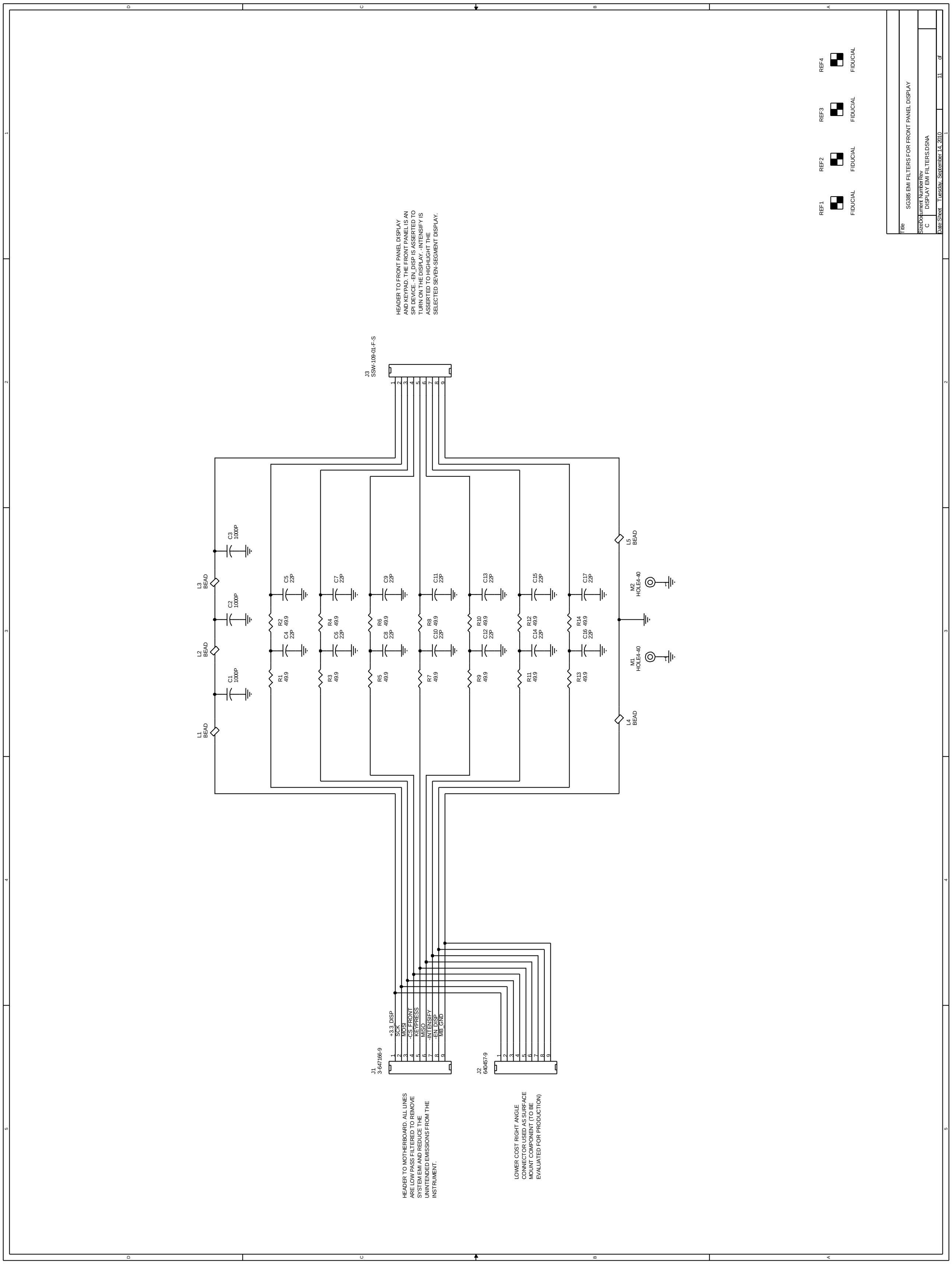
Schematic 1: Block Diagram



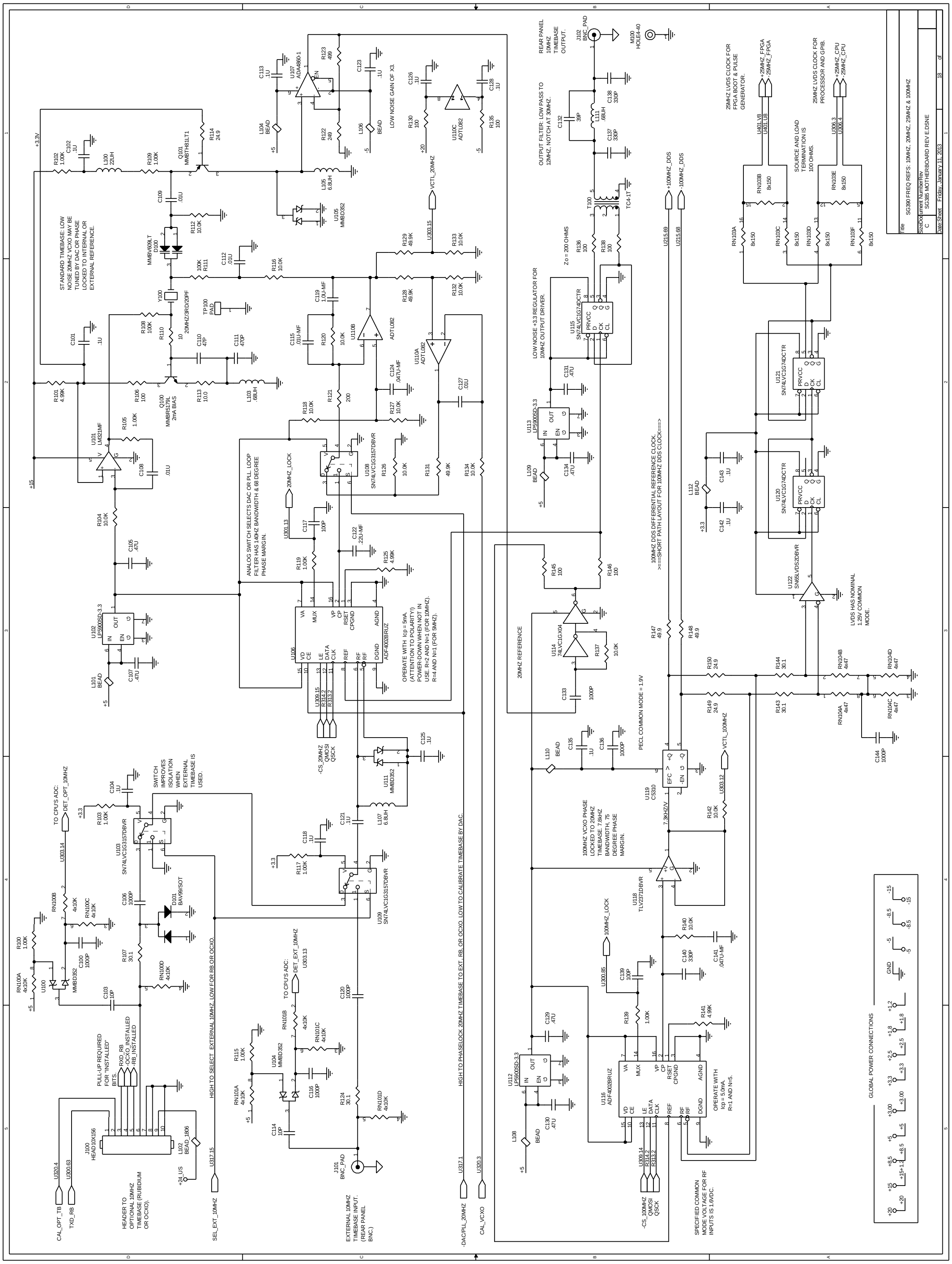
Schematic 2: Front Panel Display



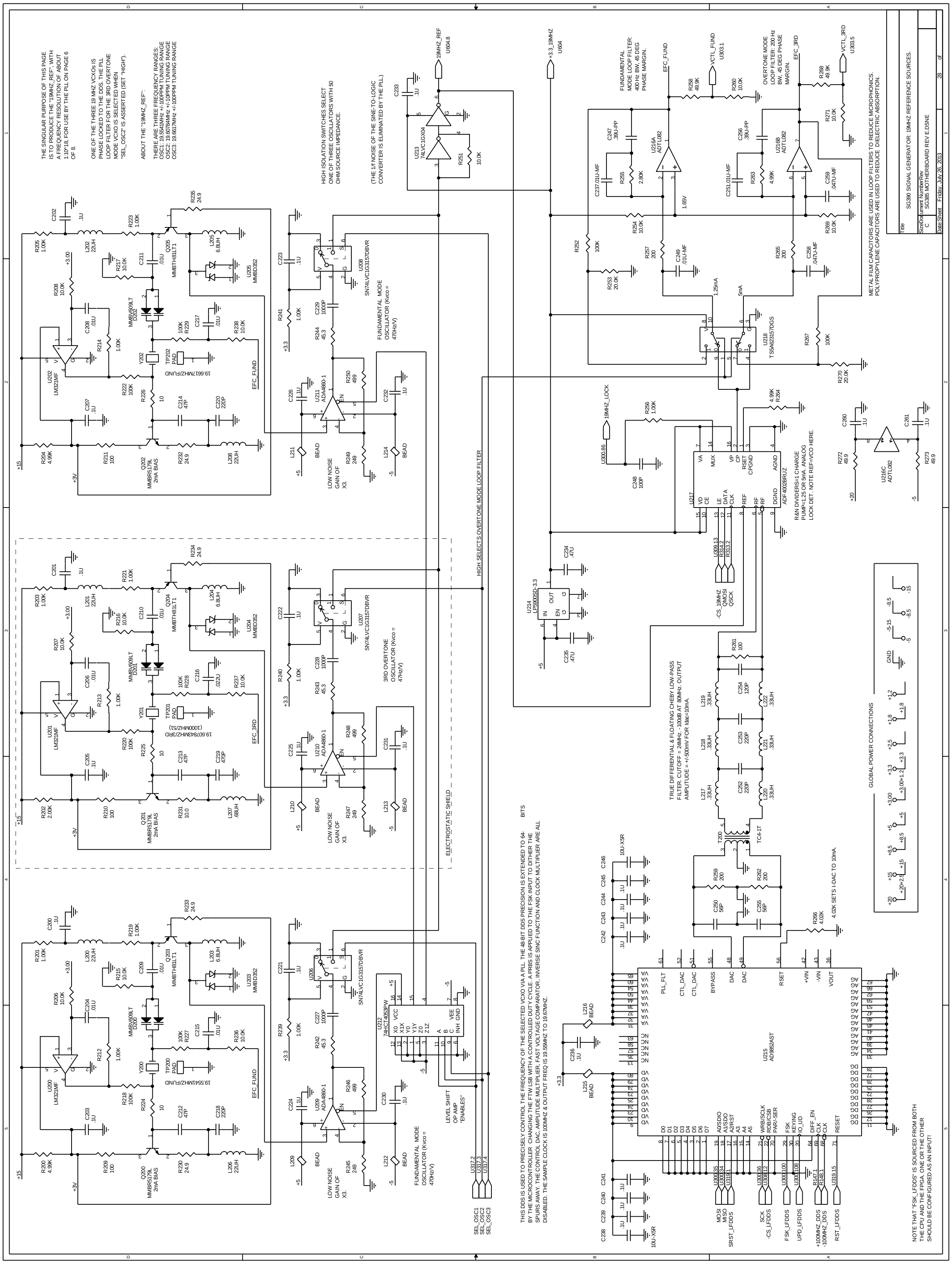
Schematic 3: Display EMI Filter



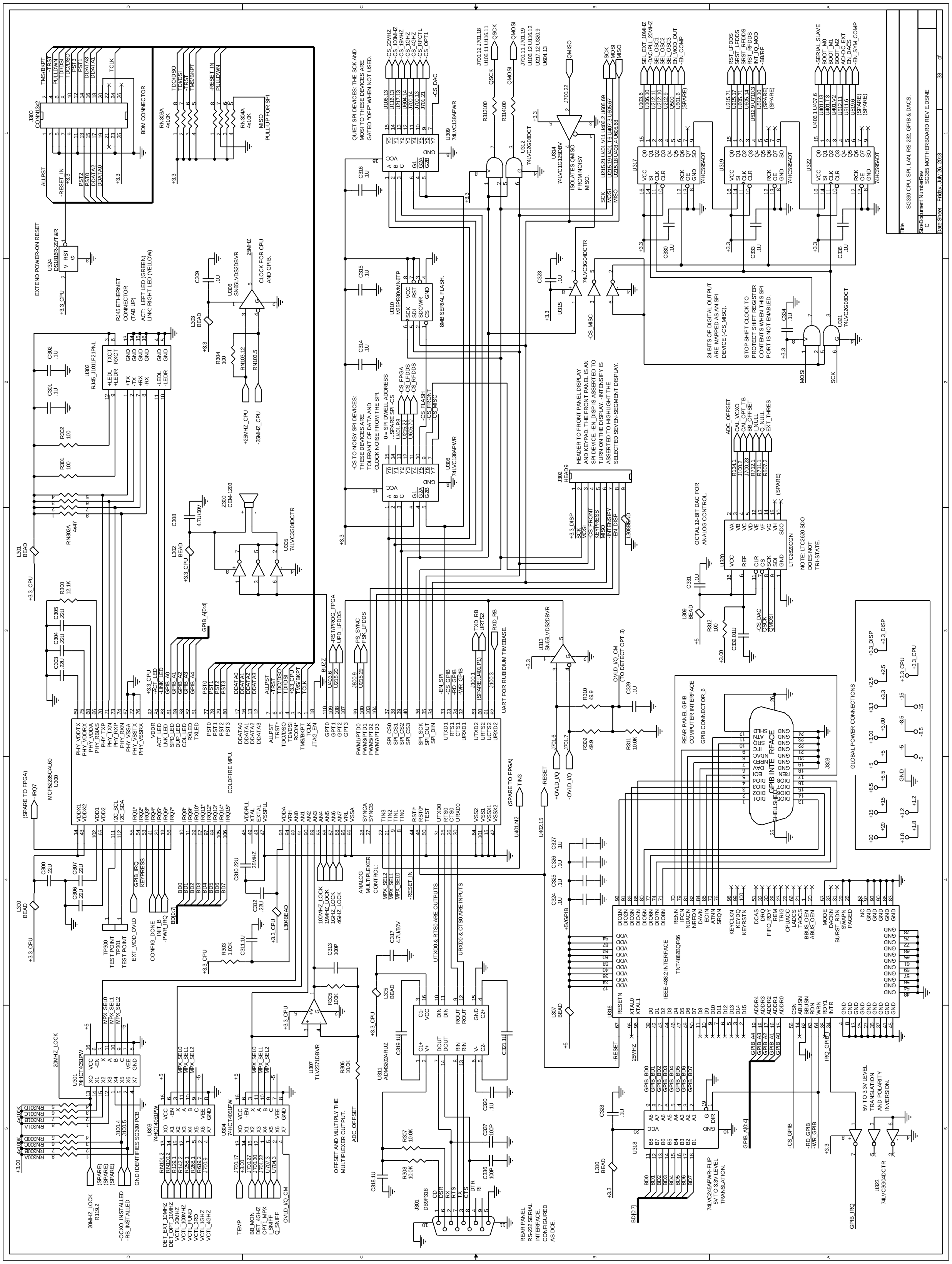
Schematic 4: Mother Board 1, Frequency Refs



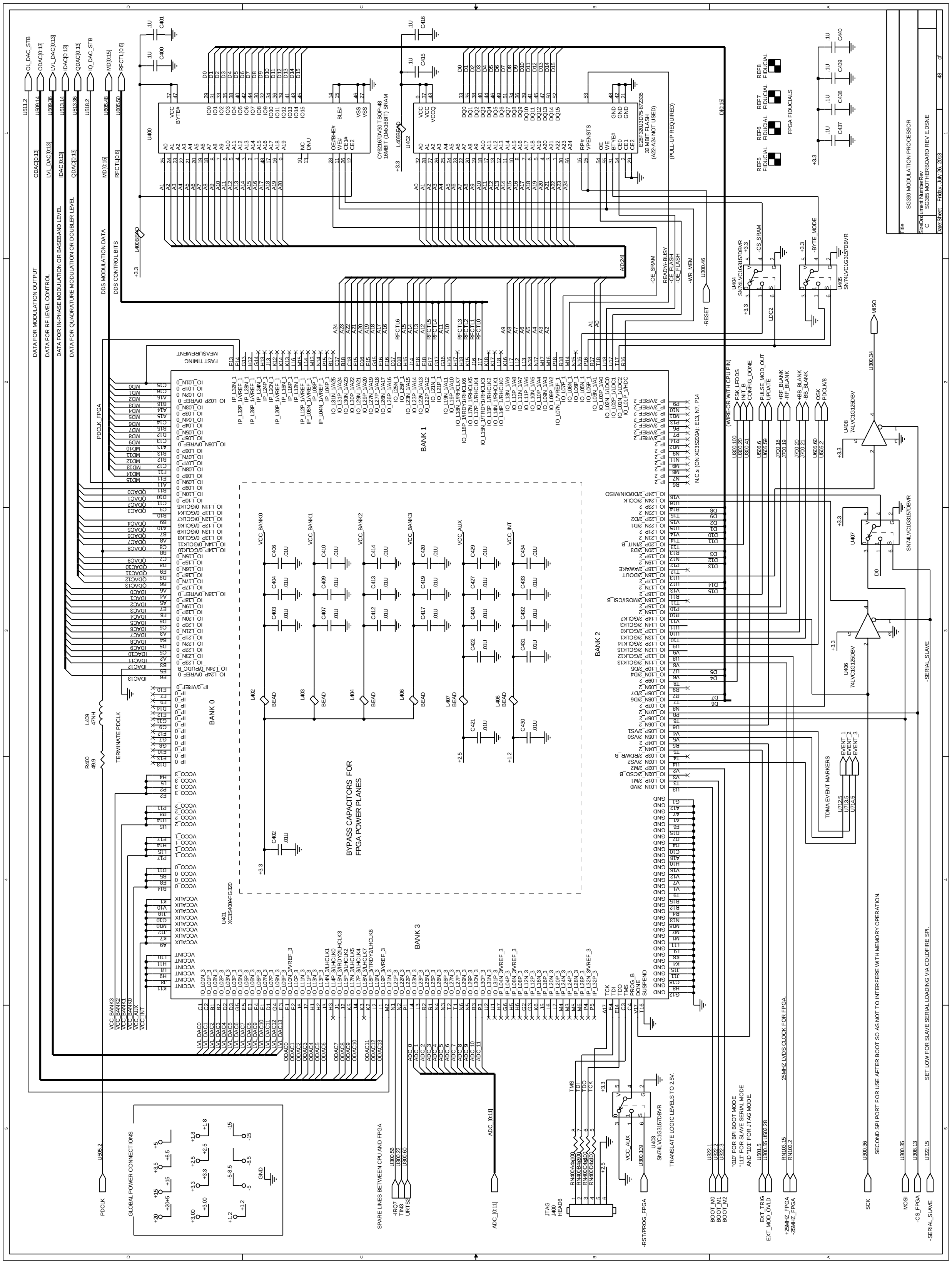
Schematic 5: Mother Board 2, 19 MHz Ref



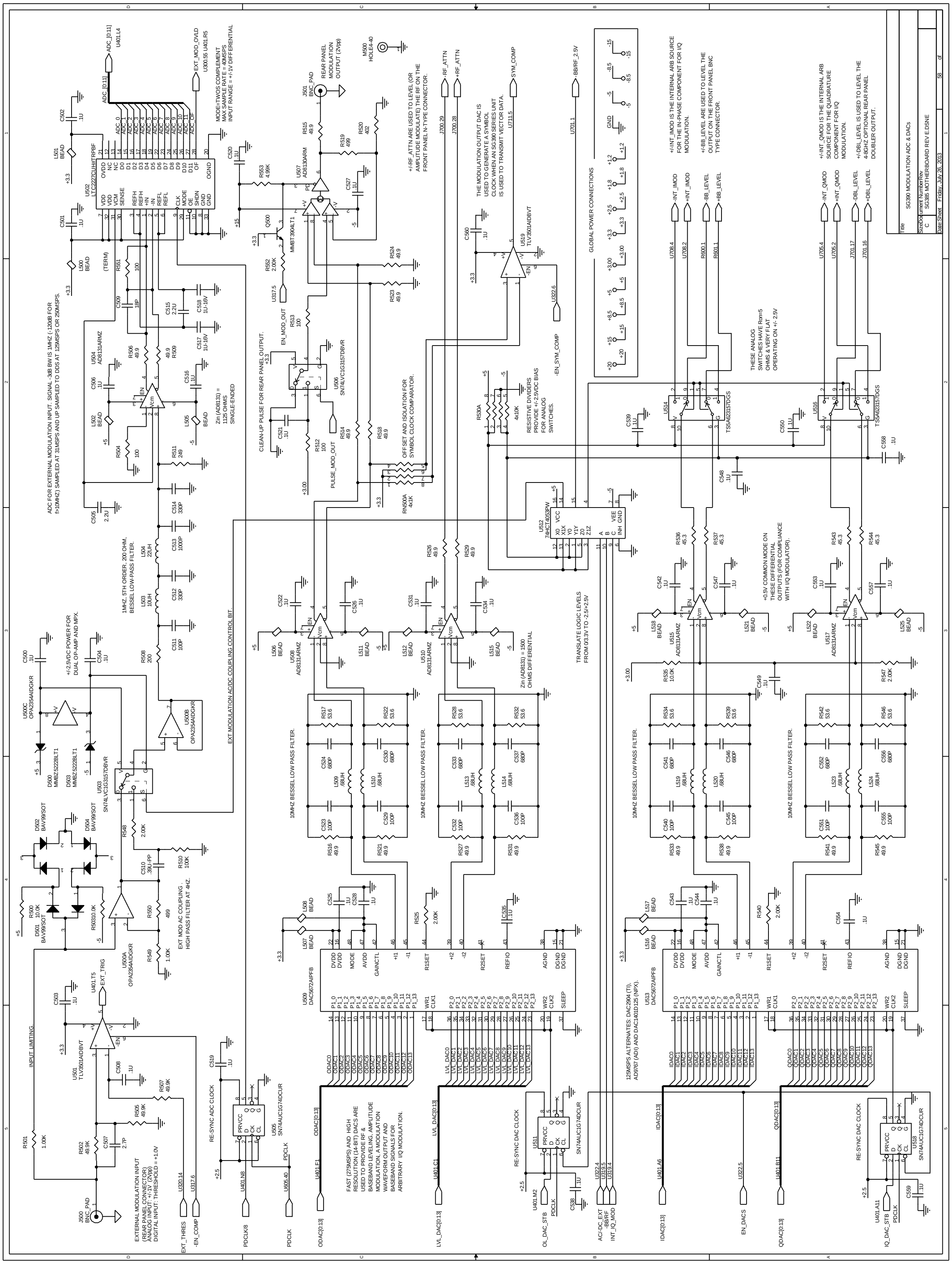
Schematic 6: Mother Board 3, CPU



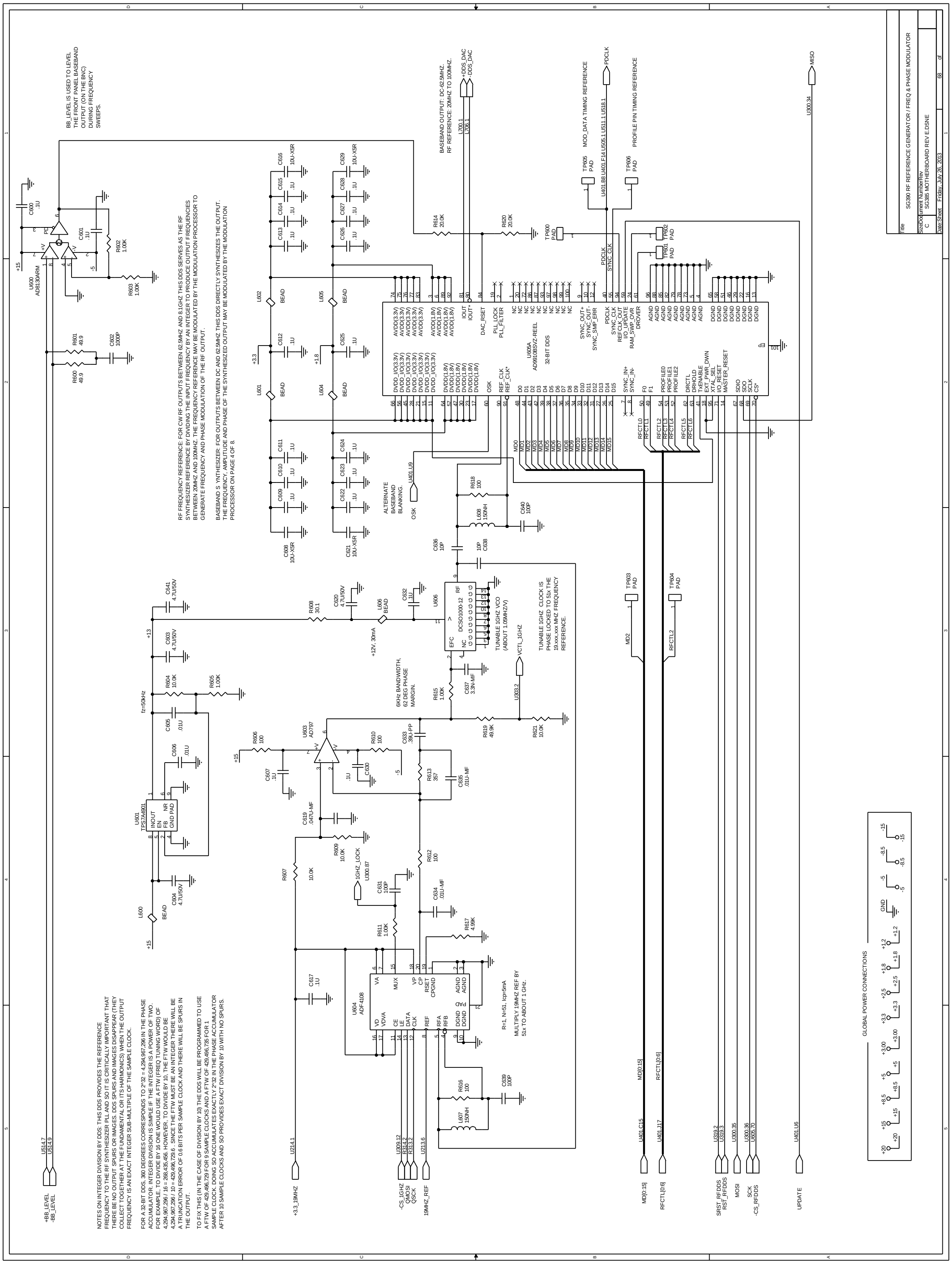
Schematic 7: Mother Board 4, Modulation Processor



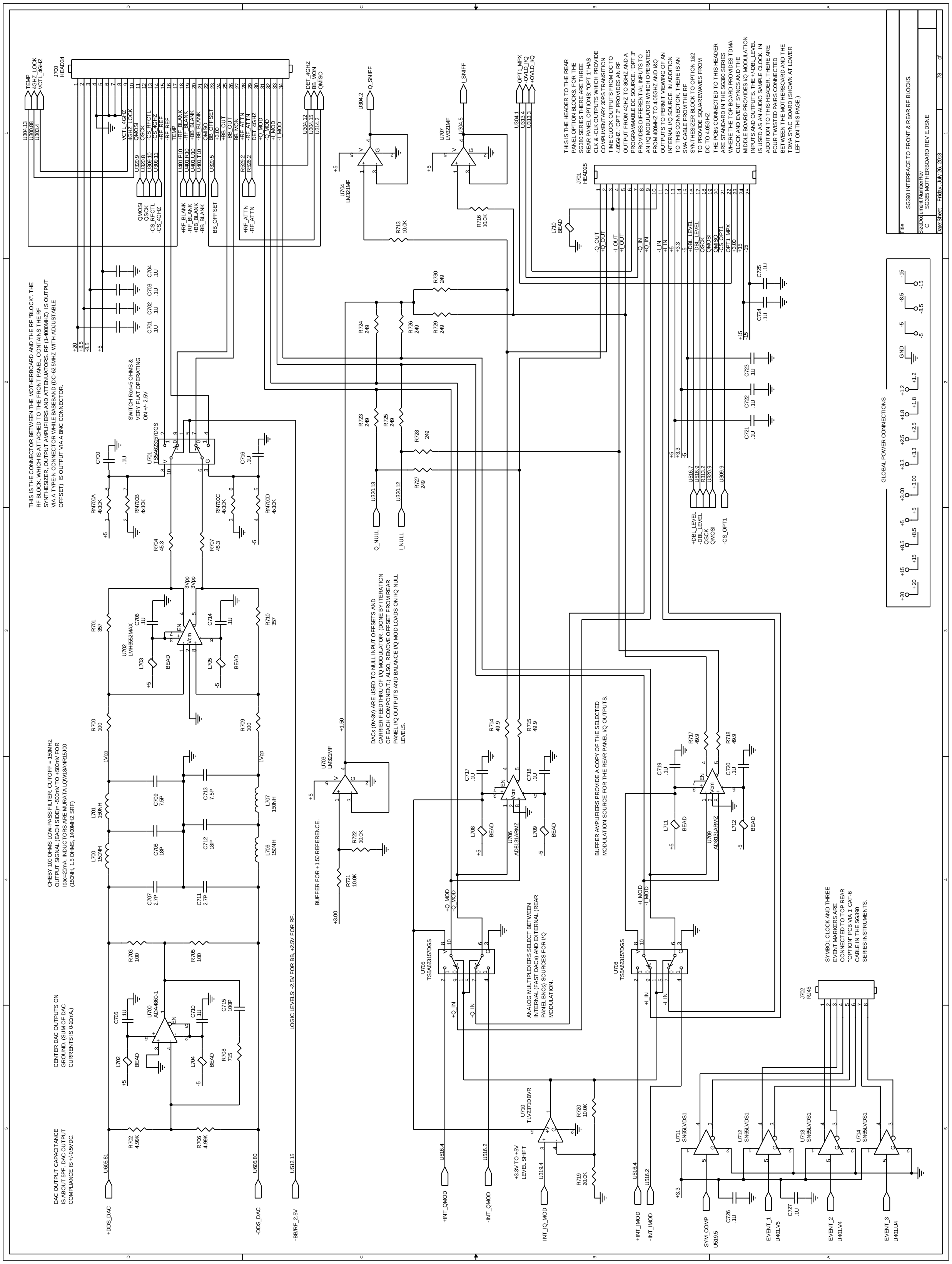
Schematic 8: Mother Board 5, Modulation ADC / DACs



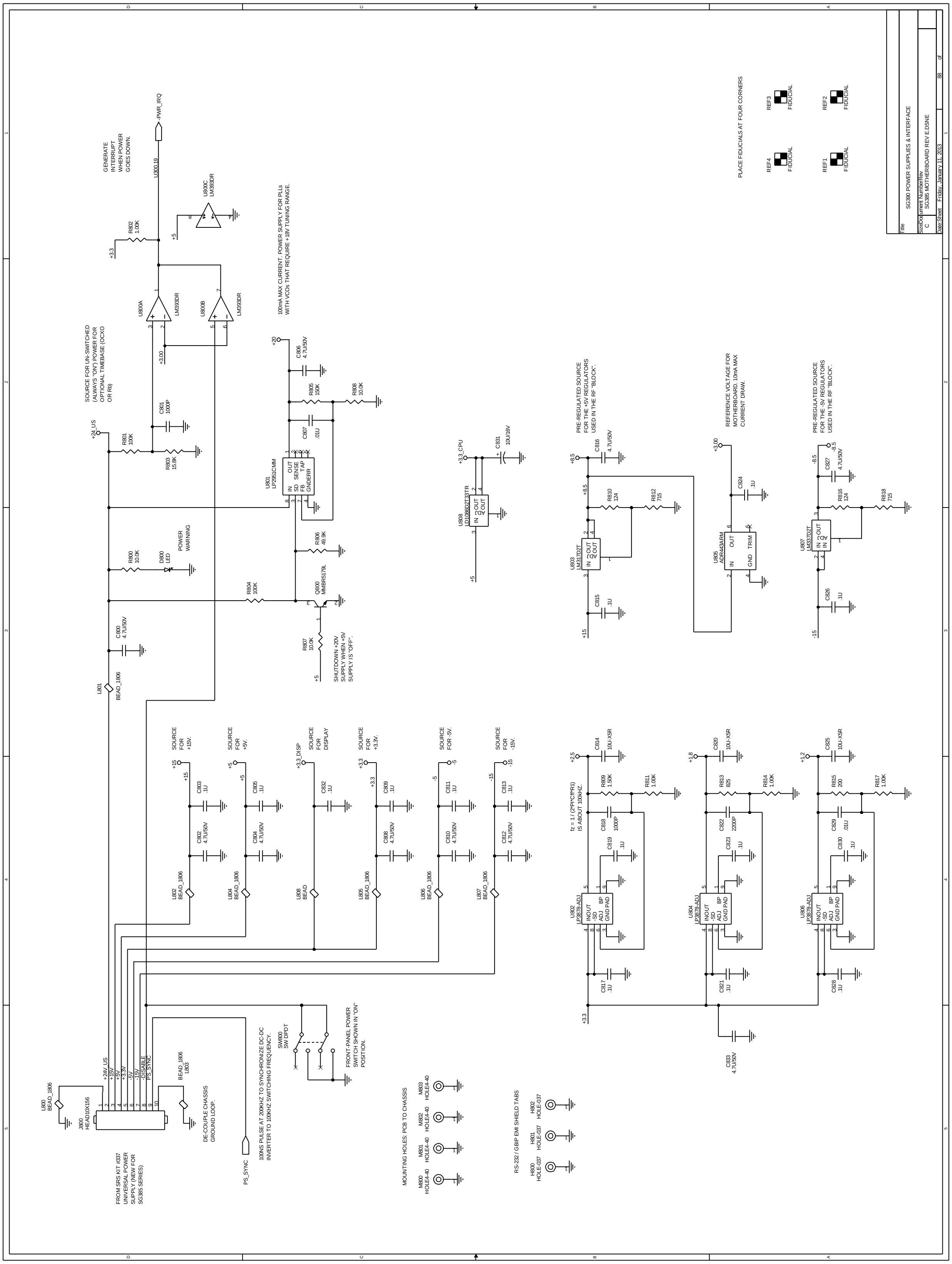
Schematic 9: Mother Board 6, RF Reference



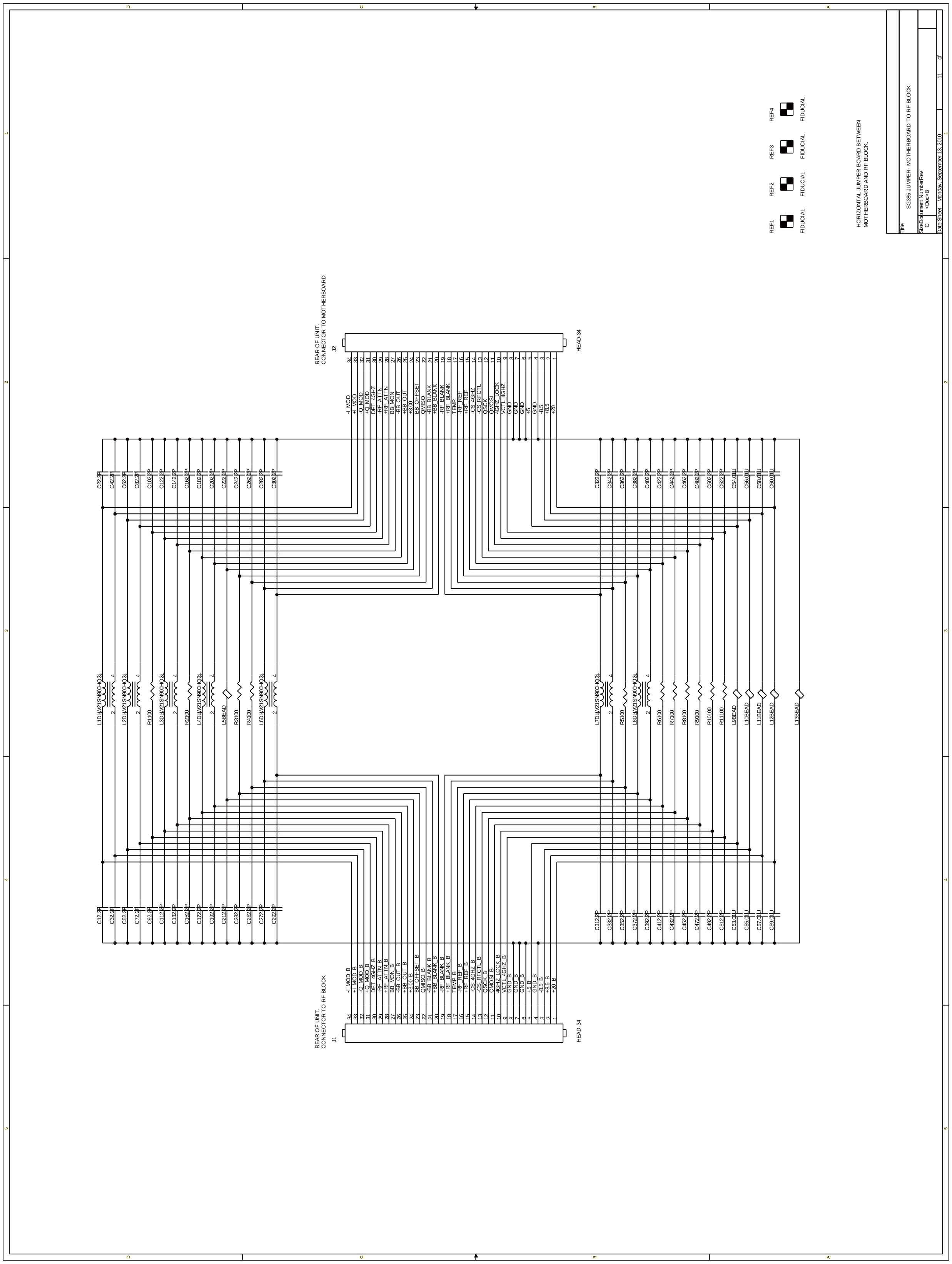
Schematic 10: Mother Board 7, Interface



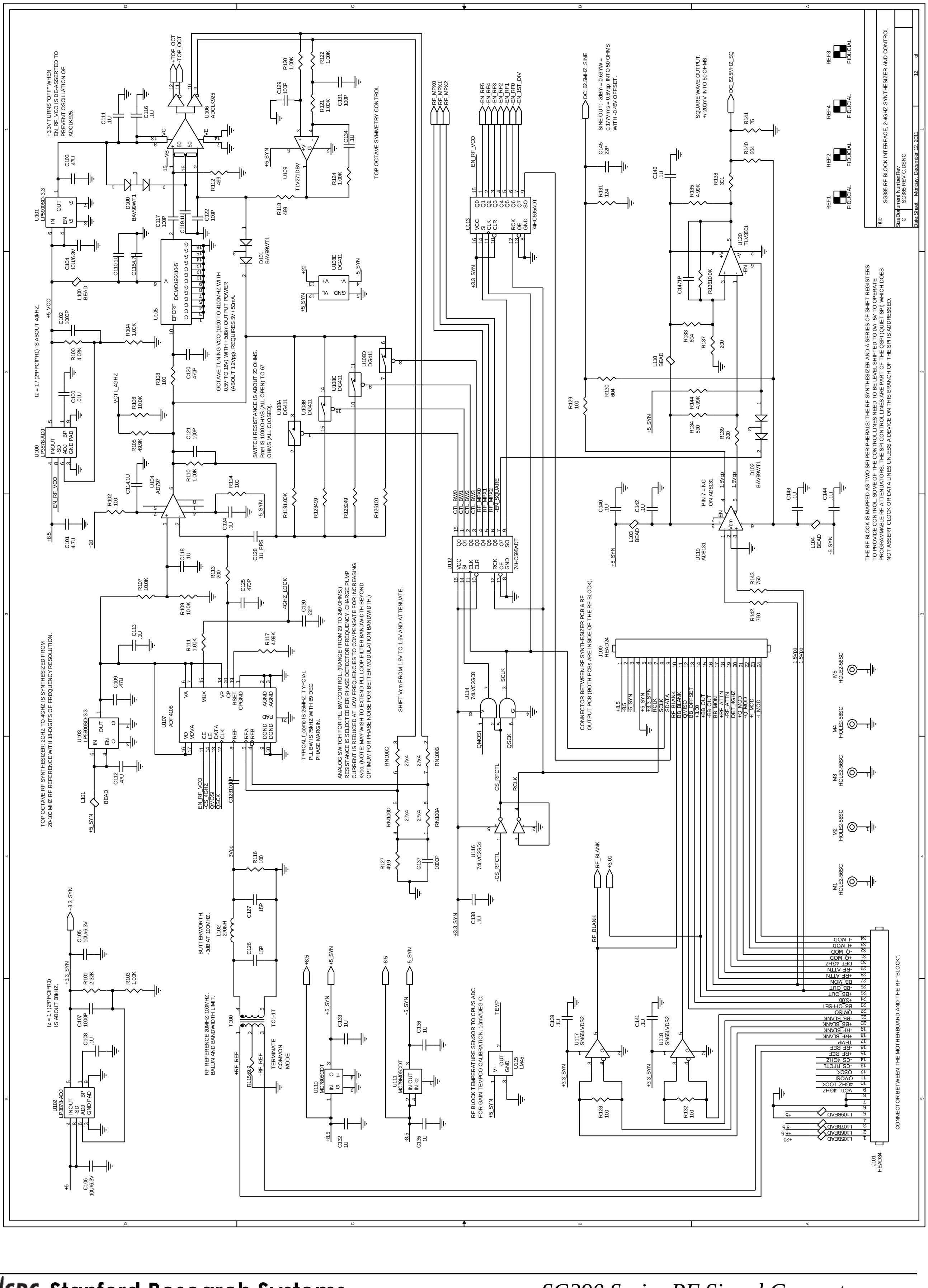
Schematic 11: Mother Board 8, Power Supplies



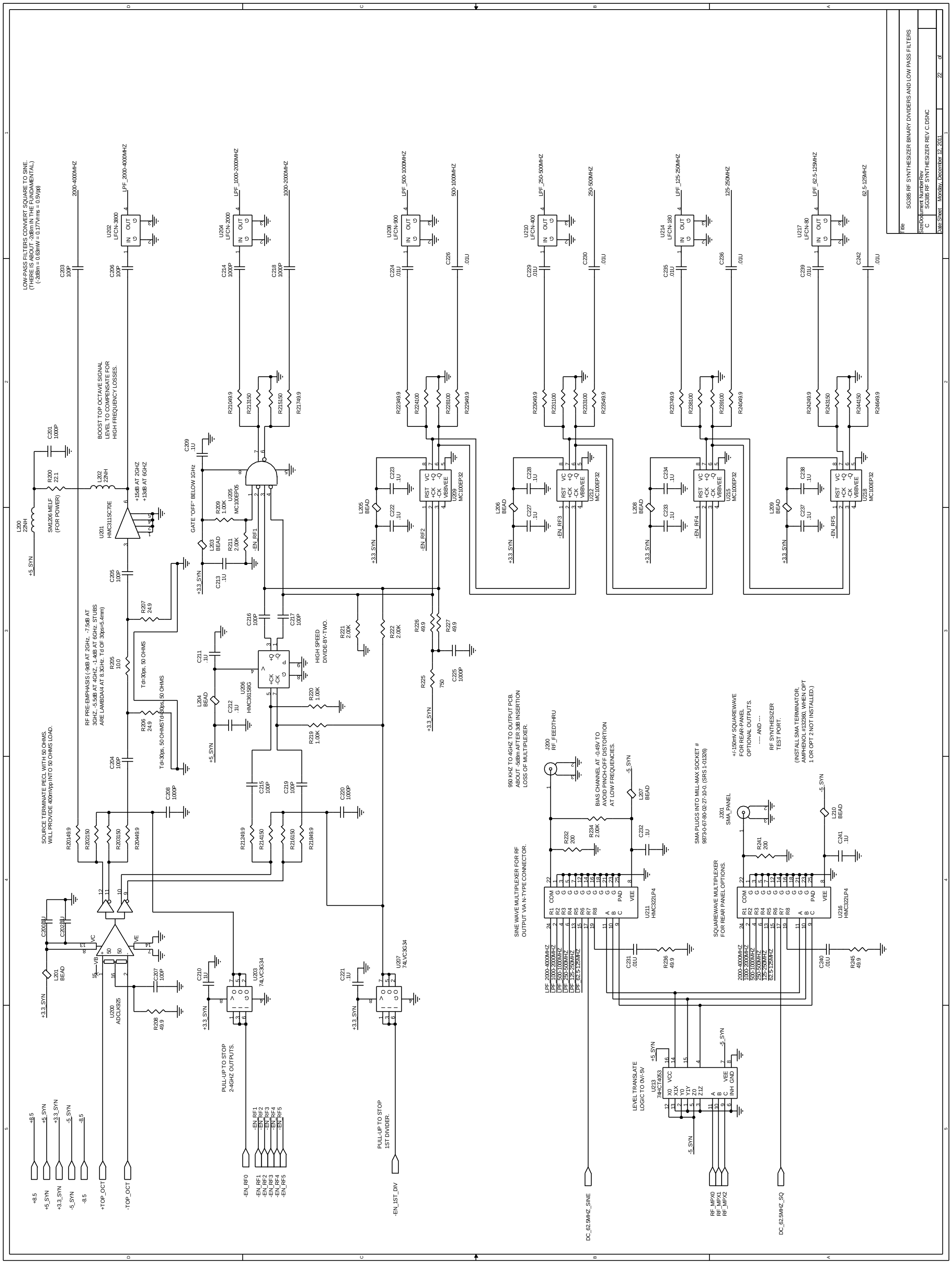
Schematic 12: Mother Board to RF Jumper



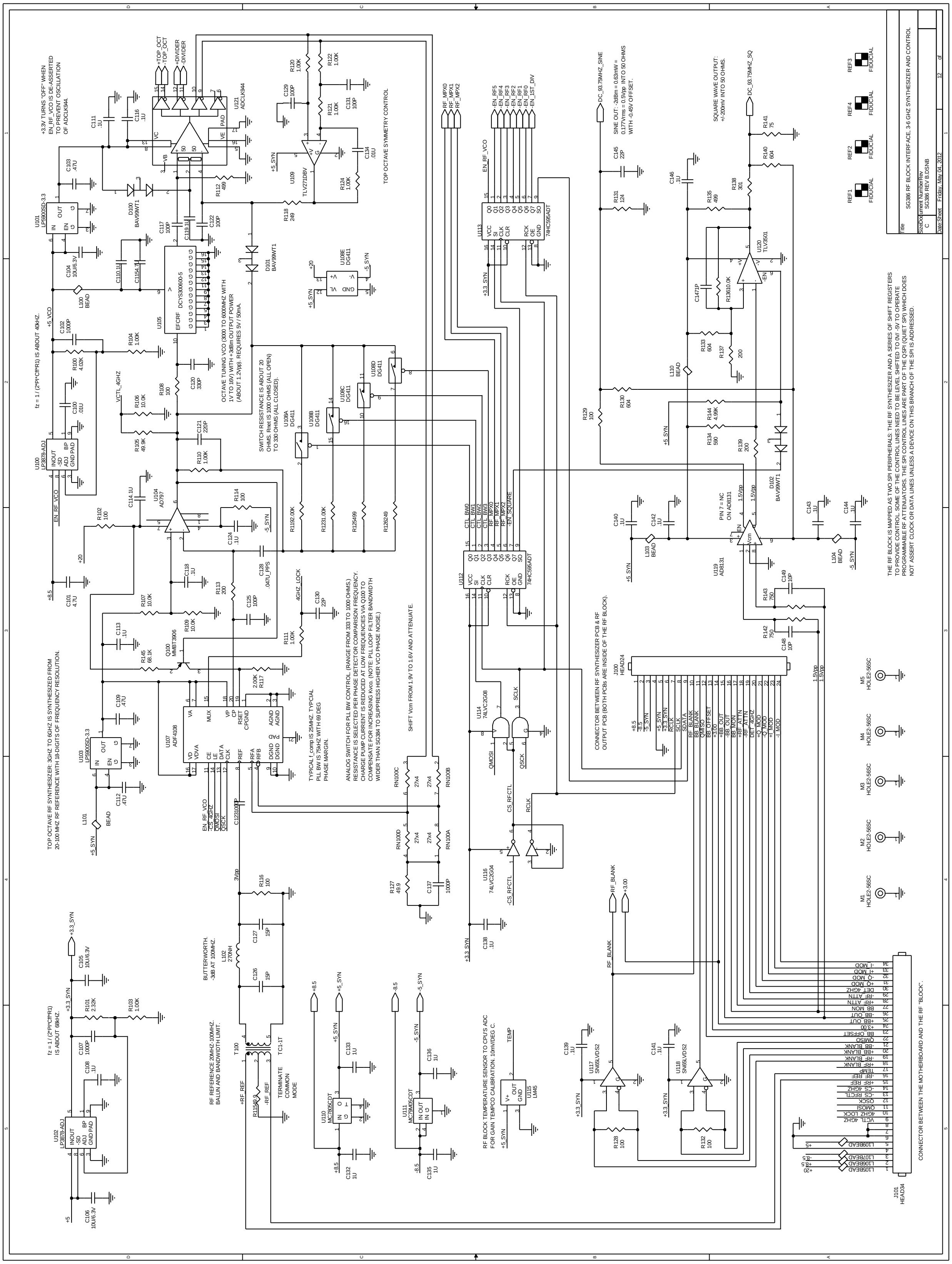
Schematic 13: SG394 Synthesizer 1, 2-4 GHz and Control



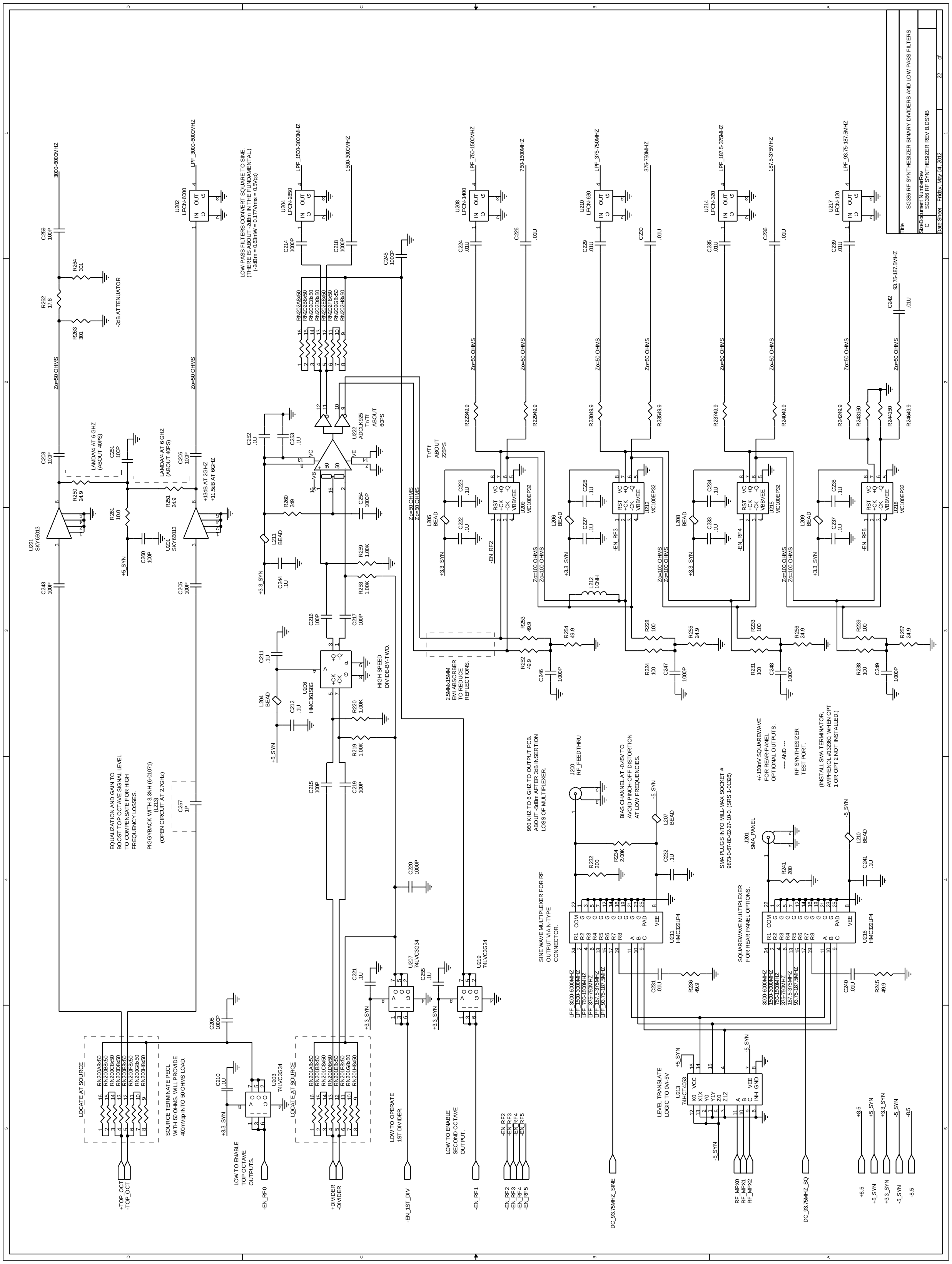
Schematic 14: SG394 Synthesizer 2, Dividers and LPF



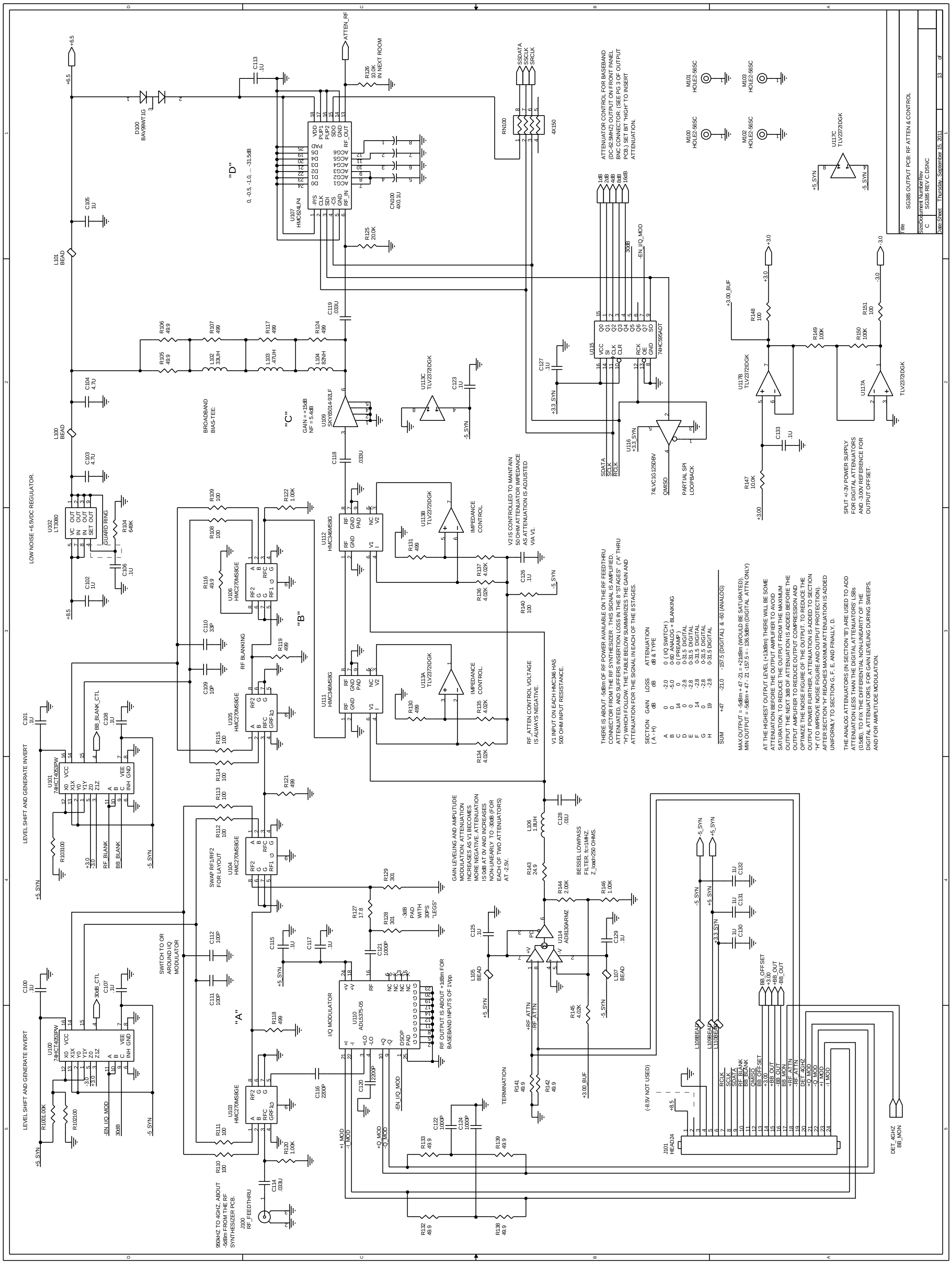
Schematic 15: SG396 Synthesizer 1, 3-6 GHz and Control



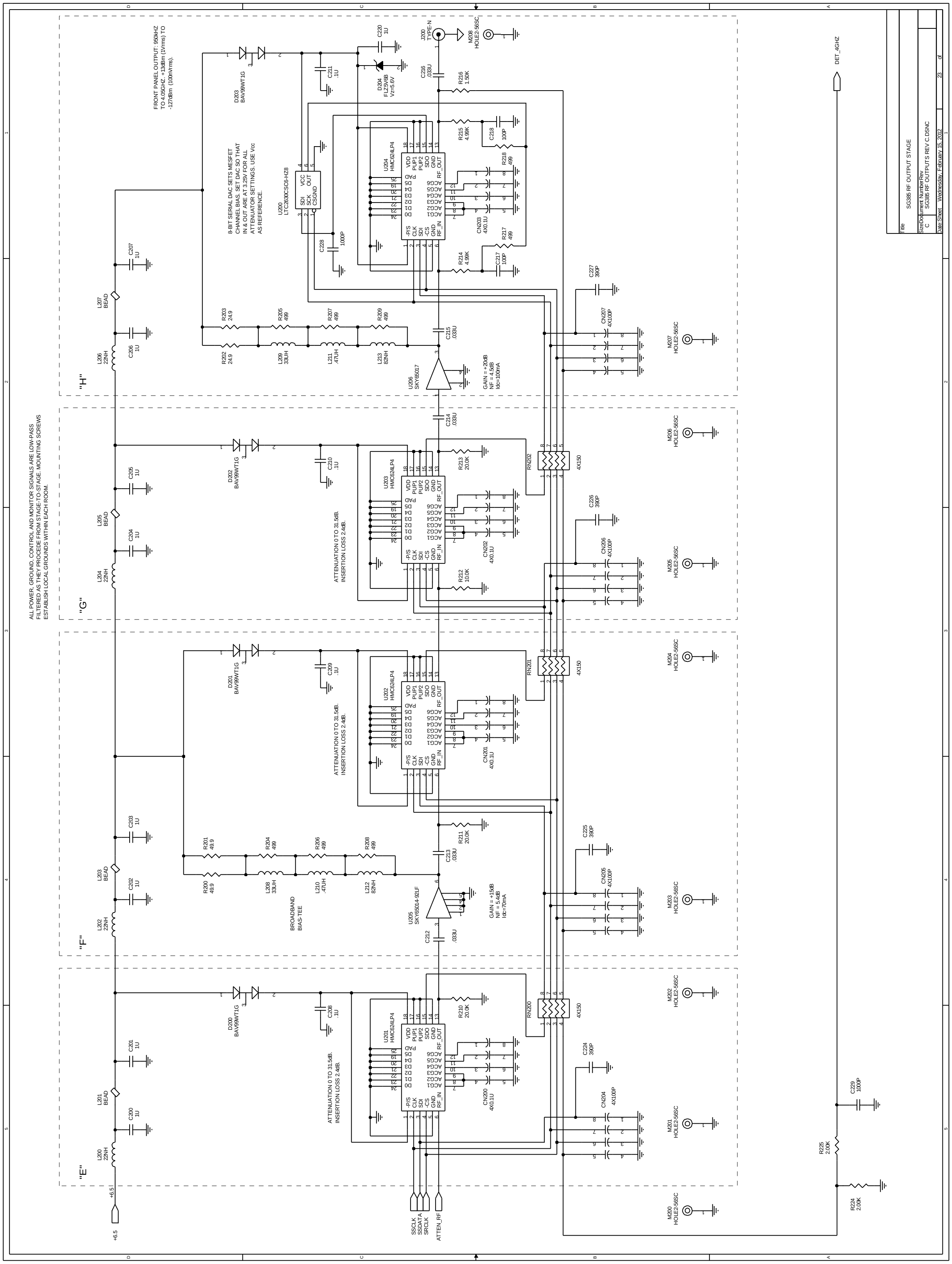
Schematic 16: SG396 Synthesizer 2, Dividers and LPF



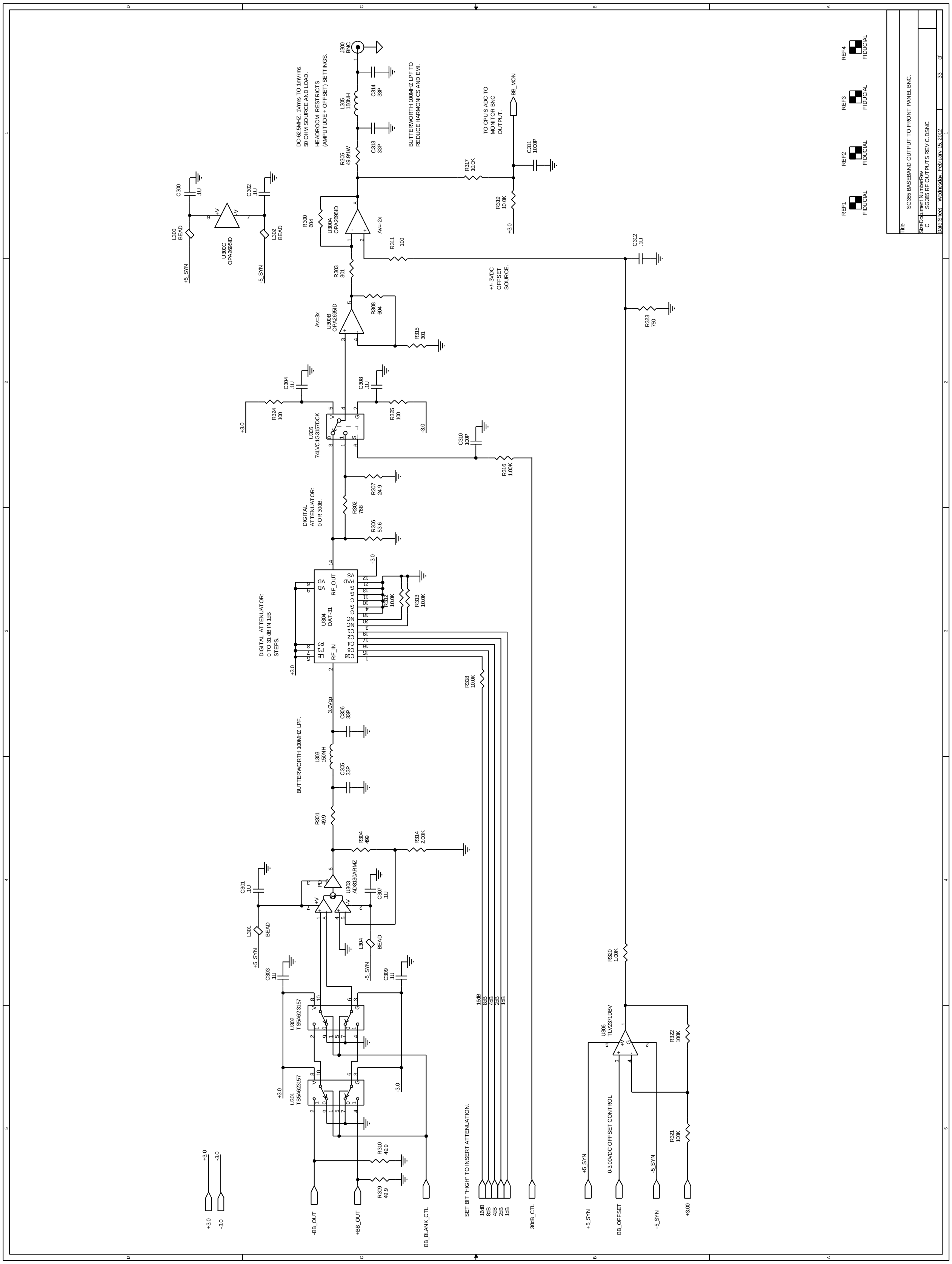
Schematic 17: SG394 Output 1, Attenuation & Controls



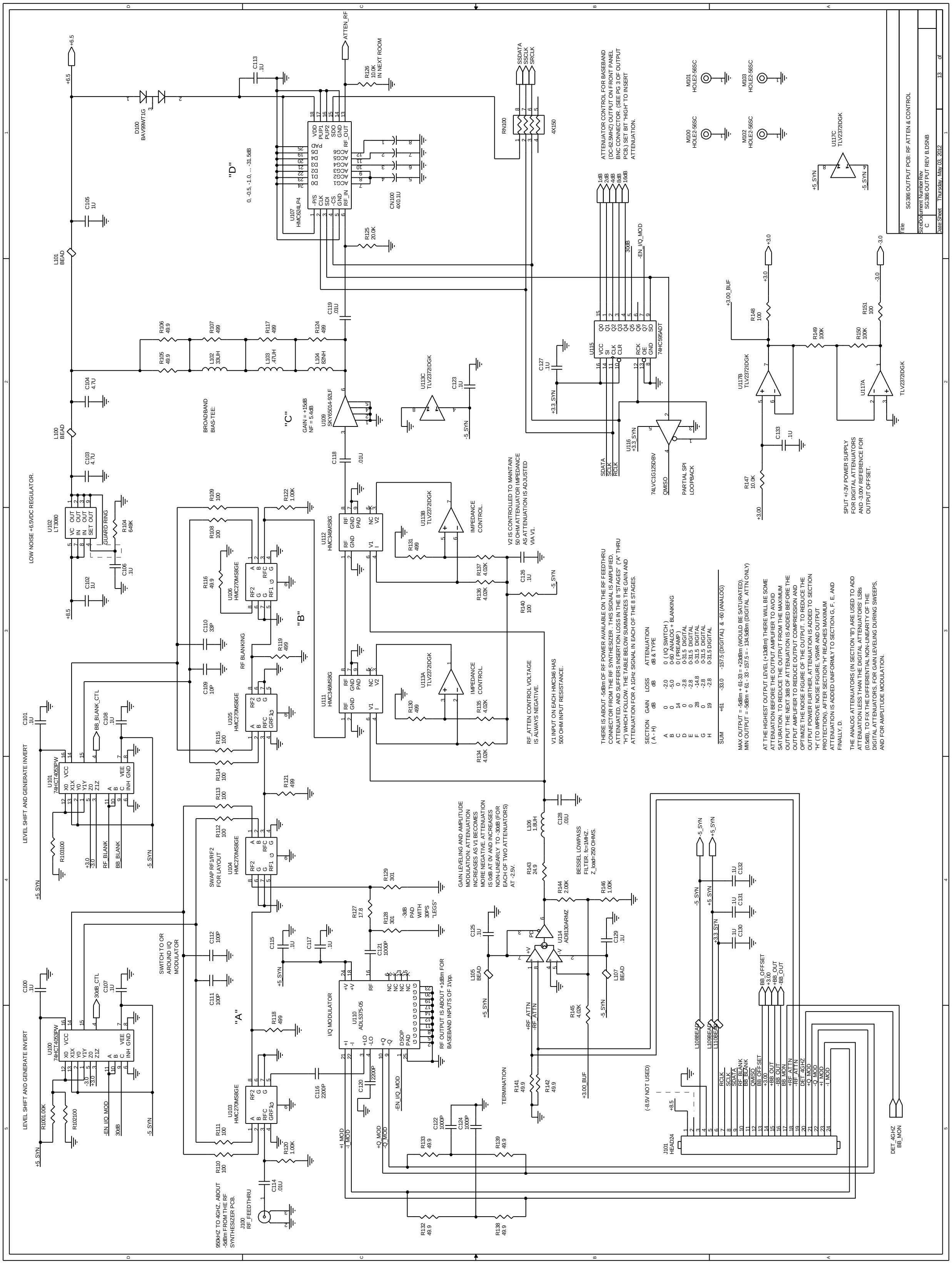
Schematic 18: SG394 Output 2, RF Stage



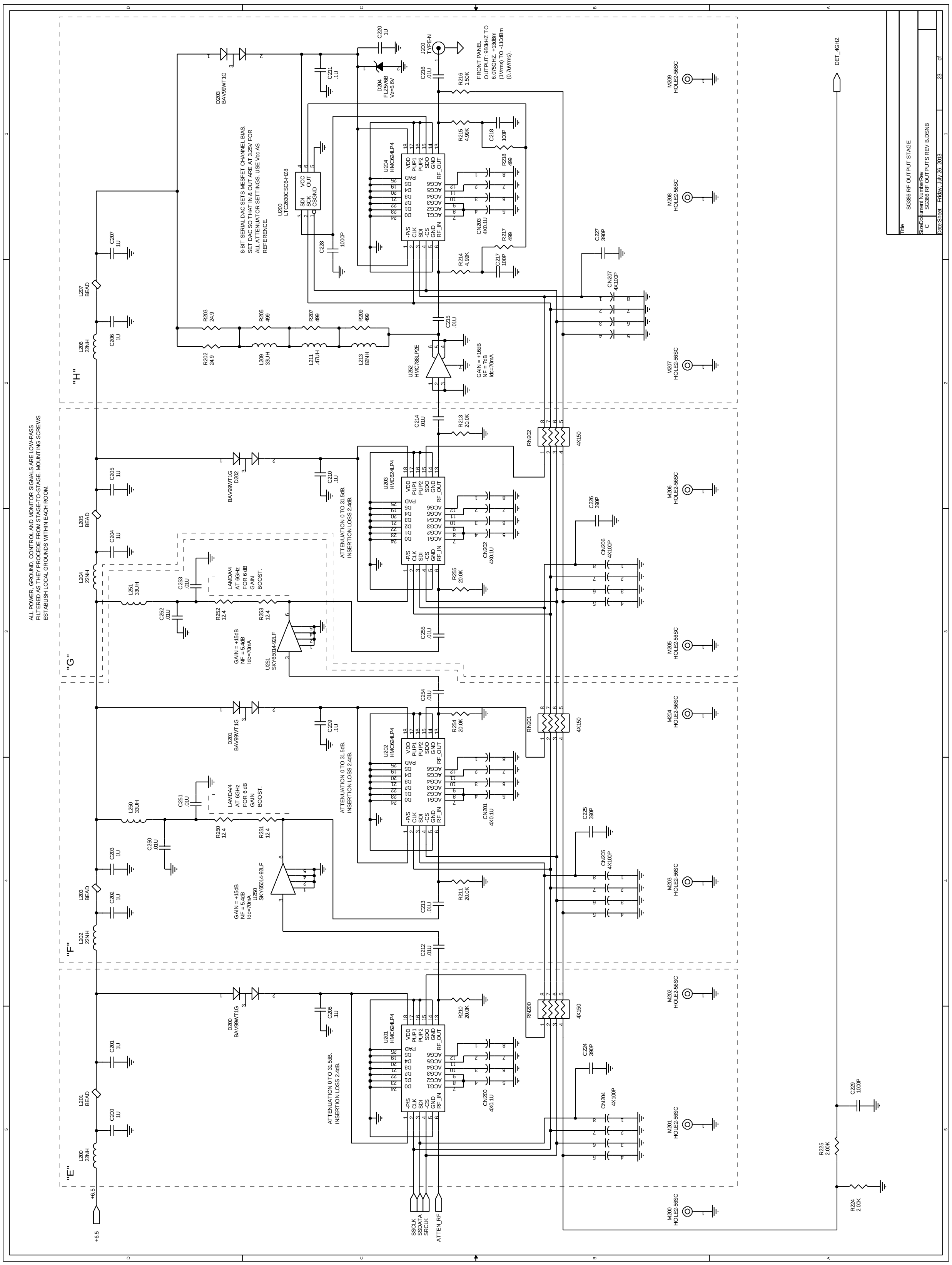
Schematic 19: SG394 Output 3, BNC



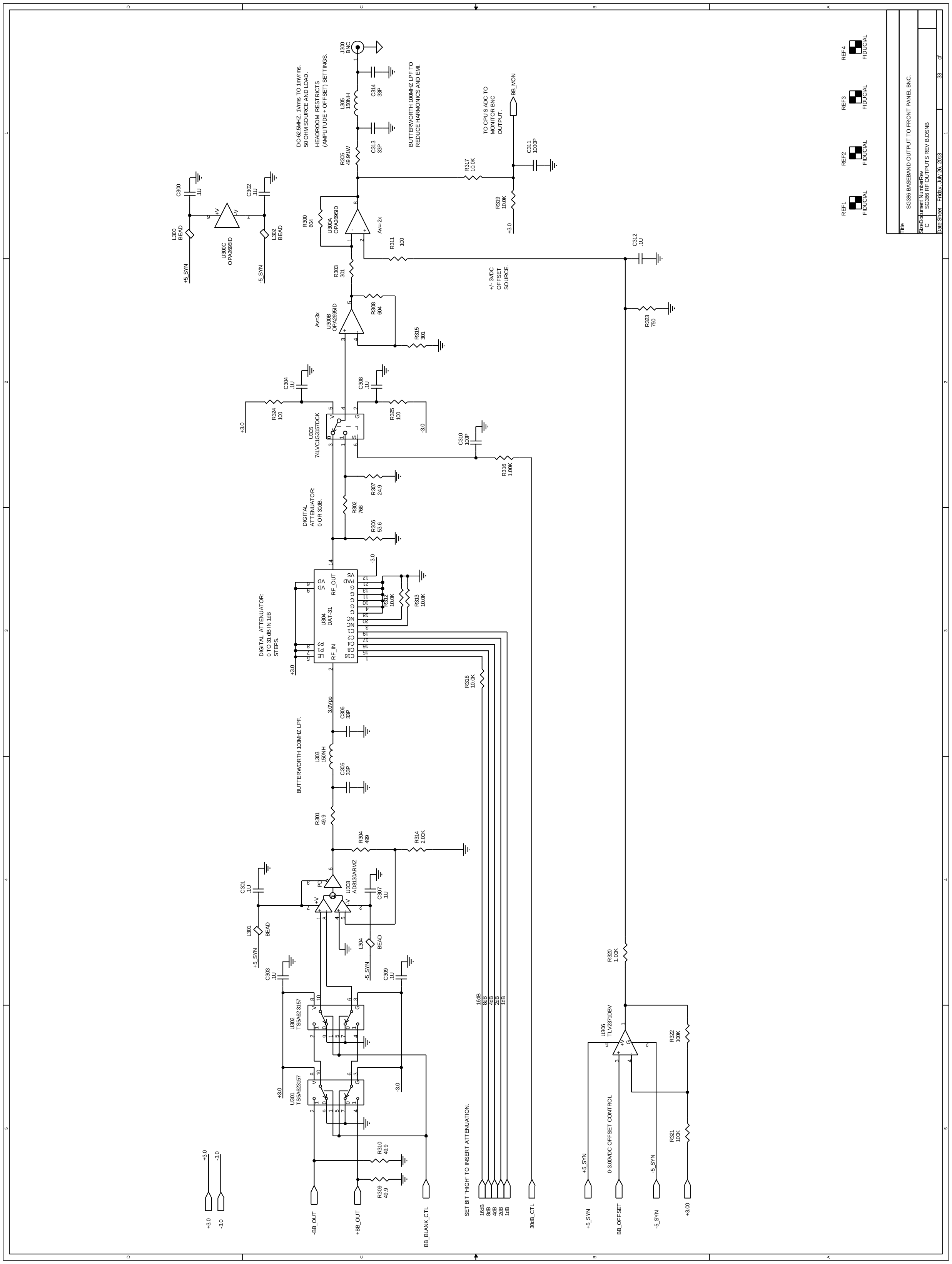
Schematic 20: SG396 Output 1, Attenuation & Controls



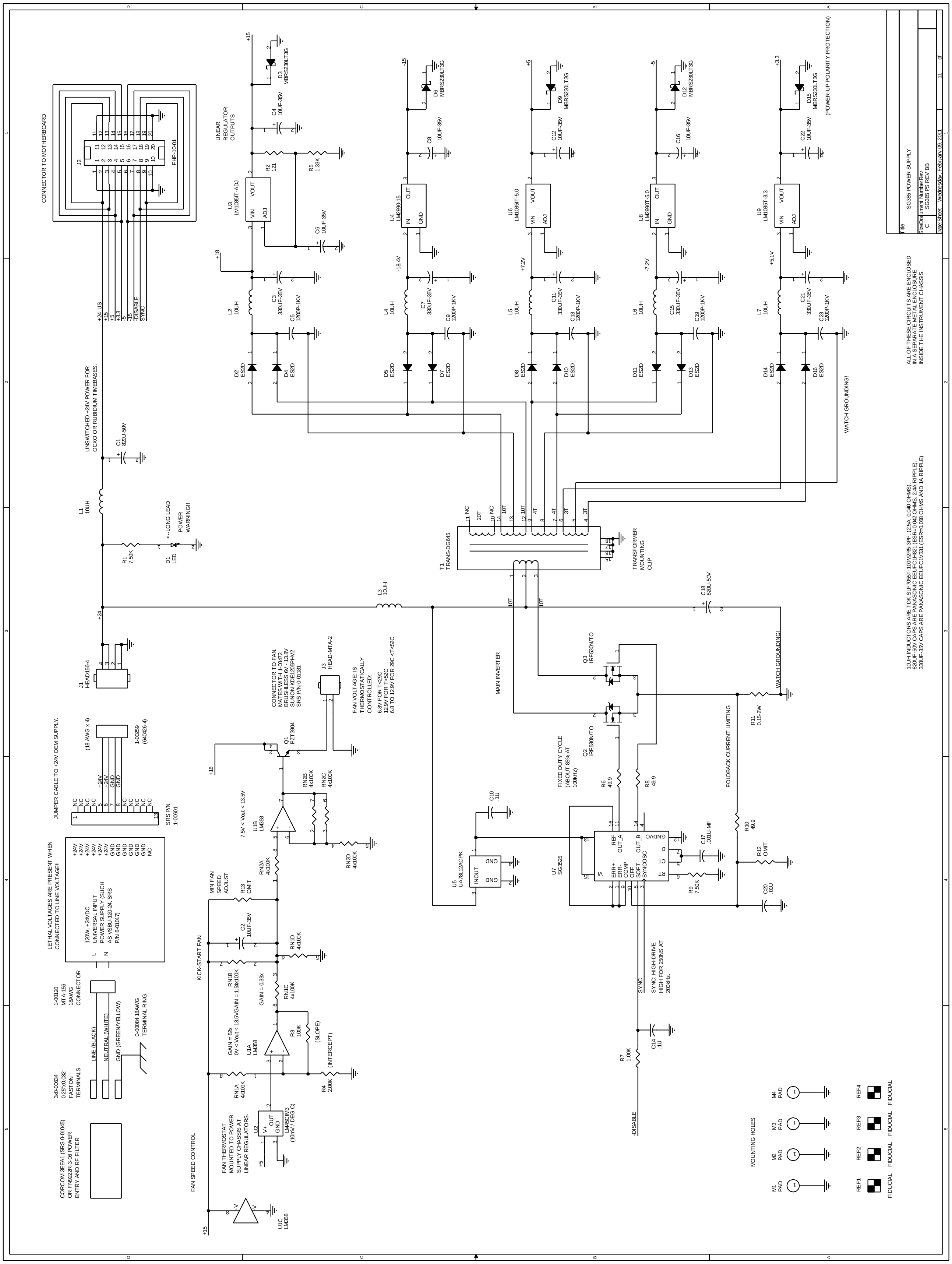
Schematic 21: SG396 Output 2, RF Stage



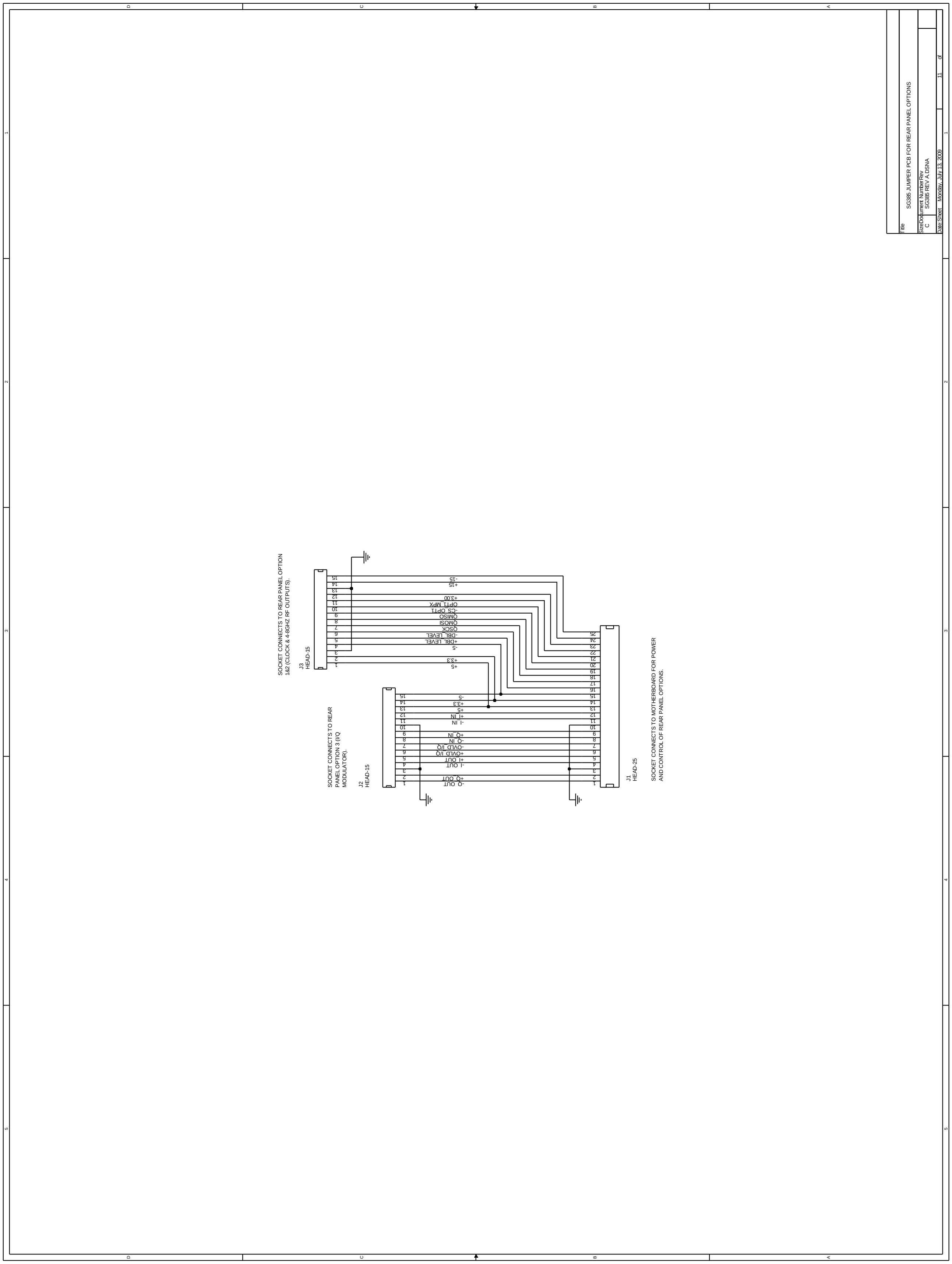
Schematic 22: SG396 Output 3, BNC



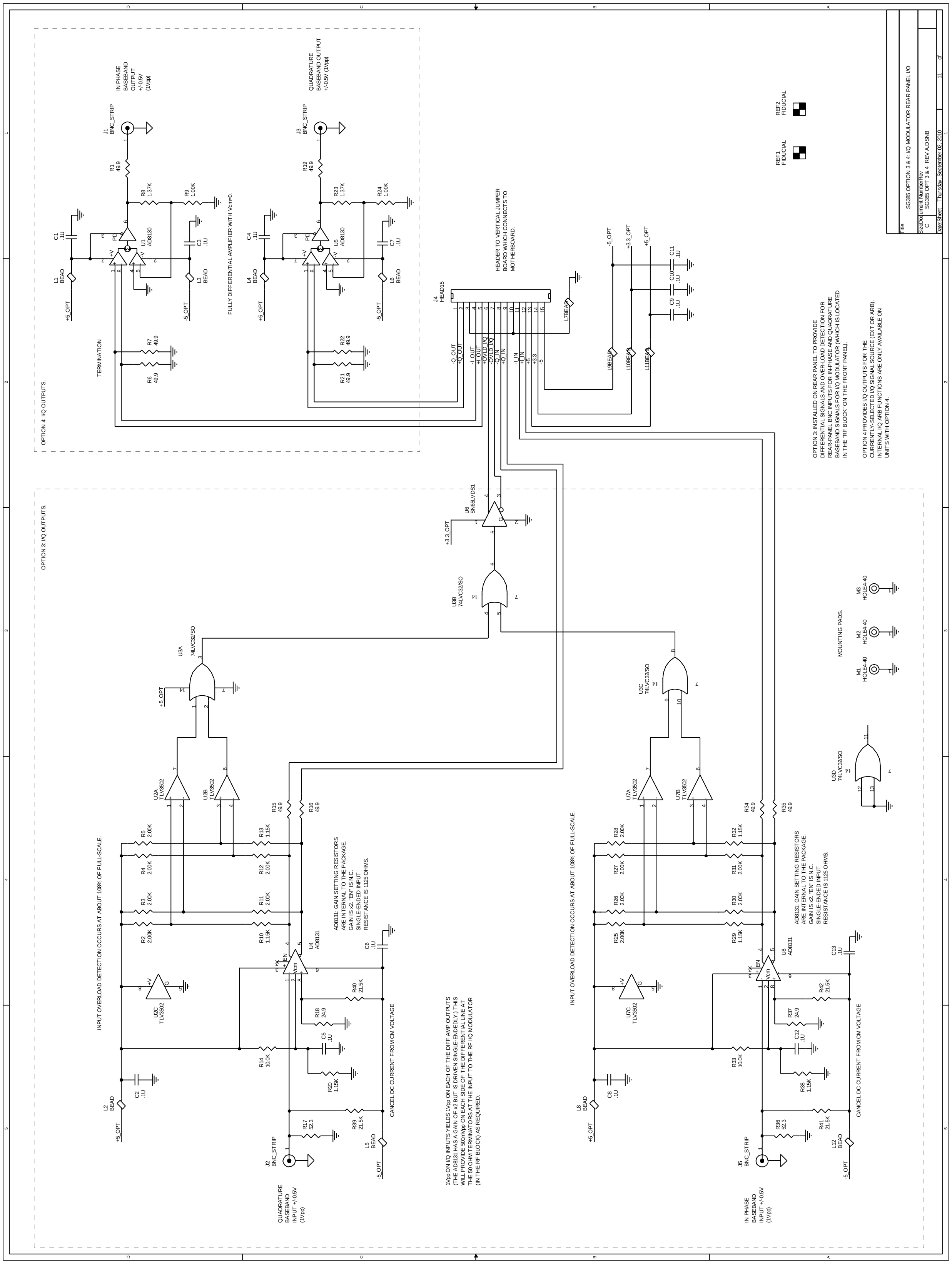
Schematic 23: Power Supply



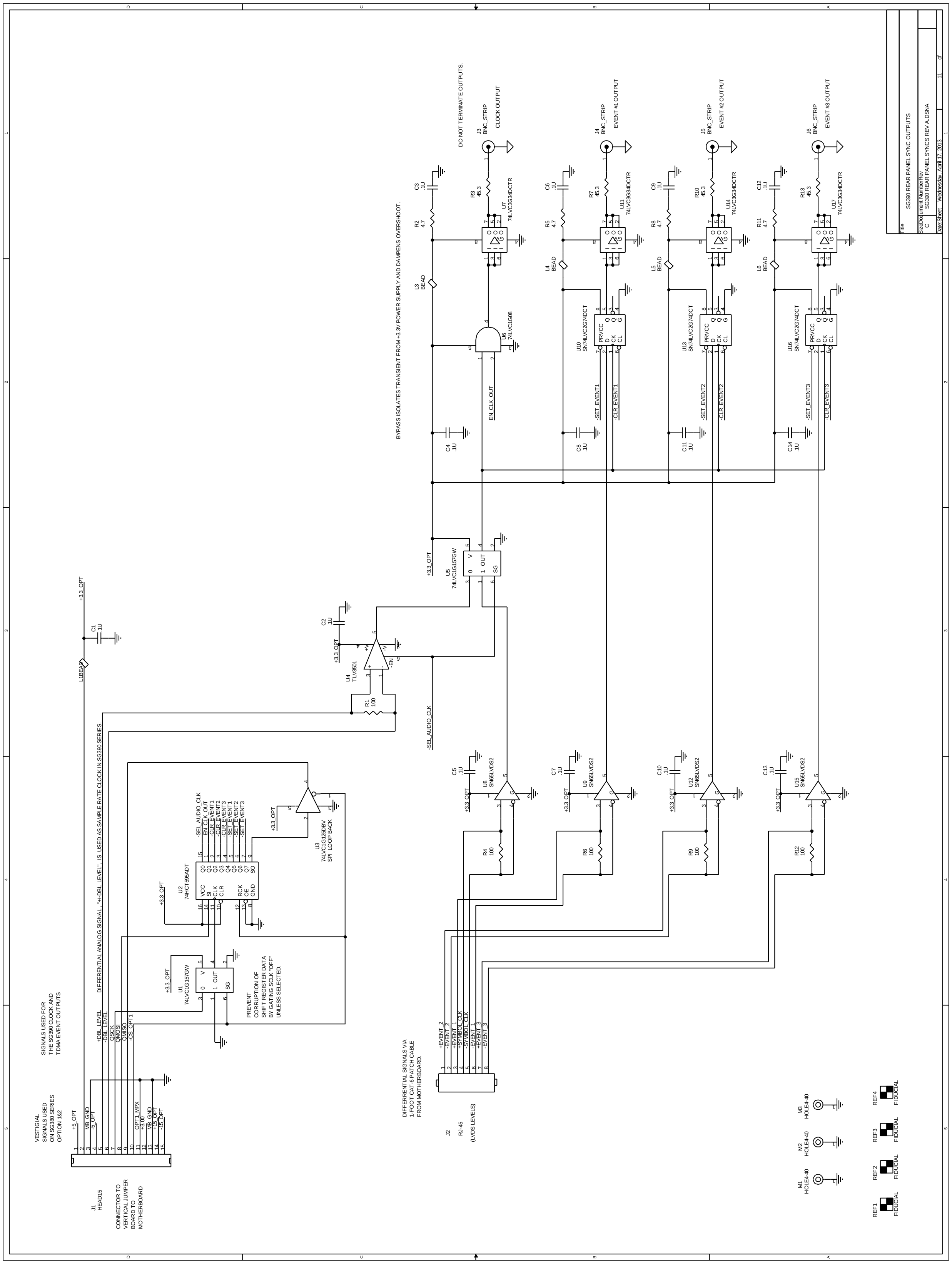
Schematic 24: Rear Panel Option Jumper



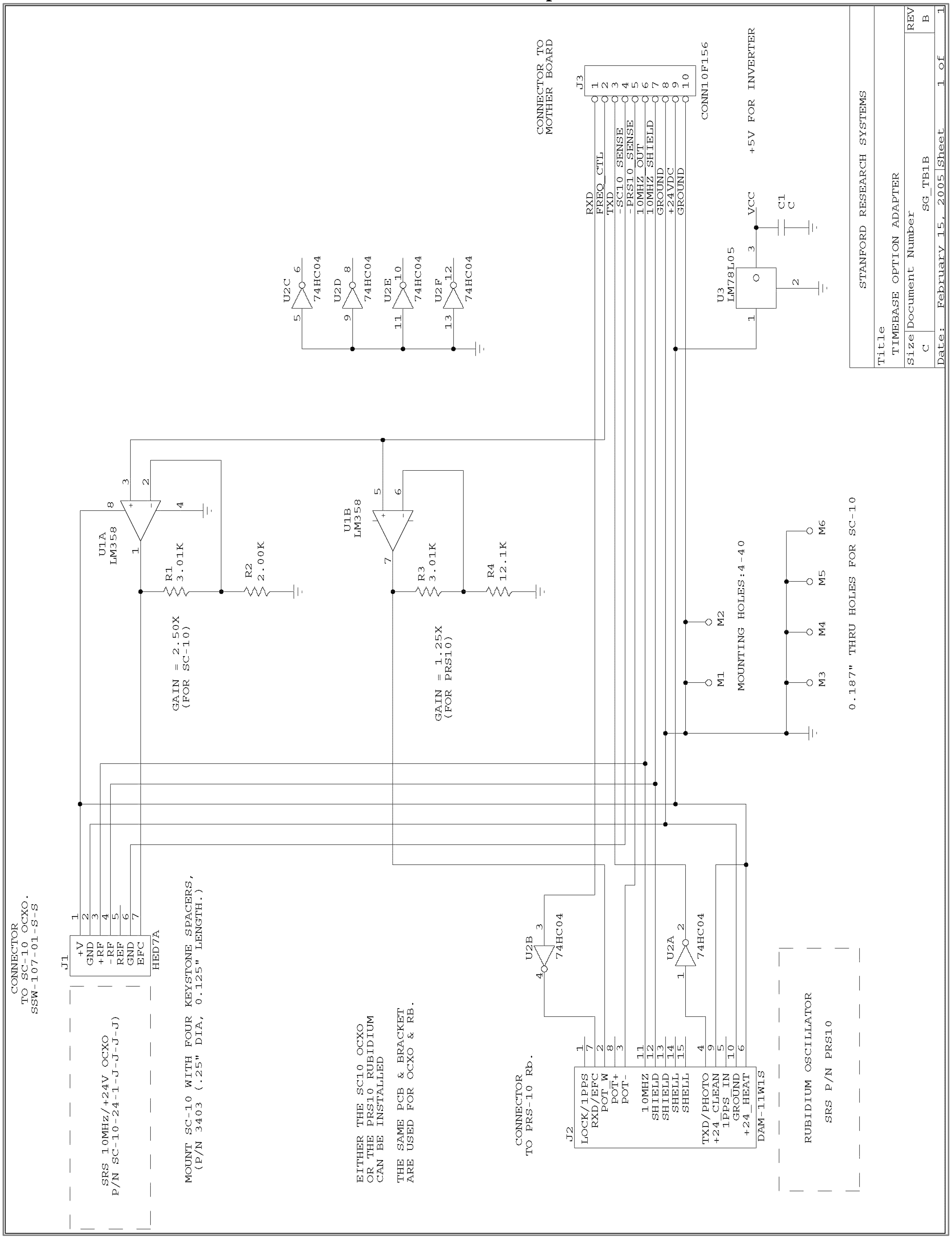
Schematic 25: I/Q Modulator



Schematic 26: Symbol Clock and Event Markers



Schematic 27: Timebase Adaptor Interface



Revisions

Rev	Date	Changes
1.00	07/26/13	First release
1.01	08/22/13	Added documentation of remote command, PTRN
1.02	09/04/13	Removed reference to Opt 2 in analog FM specification

END OF DOCUMENT